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AMERICAN SOCIETY FOR TESTING AND MATERIALS
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Standard Practice for Detection of Oxidation Induced Defects in Polished Silicon Wafers[1]

This standard is issued under the fixed designation F 1727; the number immediately following the designation indicates the year of original adoption or, in the case of revision, the year of last revision. A number in parentheses indicates the year of last reapproval. A superscript epsilon (ε) indicates an editorial change since the last revision or reapproval.

1. Scope

1.1 This practice covers the detection of crystalline defects in the surface region of silicon wafers. The defects are induced or enhanced by oxidation cycles encountered in normal device processing. An atmospheric pressure, oxidation cycle representative of bipolar, metal-oxide-silicon (MOS) and CMOS technologies is included. This practice is required to reveal strain fields arising from the presence of precipitates, oxidation induced stacking faults, and shallow etch pits. Slip is also revealed that arises when internal or edge stresses are applied to the wafer.

1.2 Application of this practice is limited to specimens that have been chemical or chemical/mechanical polished to remove surface damage from at least one side of the specimen. This practice may also be applied to detection of defects in epitaxial layers.

1.3 The surface of the specimen opposite the surface to be investigated may be damaged deliberately or otherwise treated for gettering purposes or chemically etched to remove damage.

1.4 *This standard does not purport to address all of the safety concerns, if any, associated with its use. It is the responsibility of the user of this standard to establish appropriate safety and health practices and determine the applicability of regulatory limitations prior to use.*

2. Referenced Documents

2.1 *ASTM Standards:*
D 5127 Guide for Electronic Grade Water[2]
F 1241 Terminology of Silicon Technology[3]
F 1725 Guide for Analysis of Crystallographic Perfection of Silicon Ingots[3]
F 1726 Guide for Analysis of Crystallographic Perfection of Silicon Wafers[3]
F 1809 Guide for Selection and Use of Etching Solutions to Delineate Structural Defects in Silicon[3]
F 1810 Test Method for Counting Preferentially Etched or Decorated Surface Defects in Silicon Wafers[3]

2.2 *SEMI Specifications:*[4]
SEMI C-1 Specification for Reagents
SEMI C-3 Specifications for Gases

3. Terminology

3.1 Defect-related terminology may be found in Terminology F 1241.

4. Summary of Practice

4.1 Wet oxidation is used to generate or highlight defects, or both, in silicon wafers. This oxidation may also simulate simple device production processes. The defects are revealed subsequently by preferential etching and examination by interference contrast microscopy according to referenced ASTM standards.

5. Significance and Use

5.1 Defects induced by thermal processing of silicon wafers may adversely influence device performance and yield.

5.2 These defects are influenced directly by contamination, ambient atmosphere, temperature, time at temperature, and rate of change of temperature to which the specimens are subjected. Conditions vary significantly among device manufacturing technologies. The thermal cycling procedures of this practice are intended to simulate basic device processing technologies. Oxidation cycles other than specified herein, or multiple oxidation cycles, may sometimes more accurately simulate device processing procedures. The results obtained may differ significantly from those obtained with the specified oxidation cycles.

5.3 The geometry of some patterns revealed by this practice suggests that they are related to the crystal growth process while others seem related to surface preparation or thermal cycling conditions.

5.4 This practice is suitable for acceptance testing when used with referenced practices and methods.

6. Interferences

6.1 Material having residual work damage in the polished surface exhibits visible patterns when the procedures of this practice are used. Usually, edge damage, lapping damage, tool

[1] This practice is under the jurisdiction of ASTM Committee F-1 on Electronics and is the direct responsibility of Subcommittee F01.06 on Silicon Materials and Process Control.

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[2] *Annual Book of ASTM Standards*, Vol 11.01.

[3] *Annual Book of ASTM Standards*, Vol 10.05.

[4] Available from Semiconductor Equipment and Materials International, 805 E Middlefield Rd., Mountain View, CA 94043.