
Electrostatics - Part 3-1: Methods for simulation of electrostatic effects - Human body model (HBM) - Component testing

Electrostatics -- Part 3-1: Methods for simulation of electrostatic effects - Human body model (HBM) - Component testing

Elektrostatik -- Teil 3-1: Verfahren zur Simulation elektrostatischer Entladung - Human body model (HBM) - Bauelementprüfung

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ICS:

17.220.99	Drugi standardi v zvezi z električno in magnetizmom	Other standards related to electricity and magnetism
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SIST EN 61340-3-1:2002**en**

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EUROPEAN STANDARD

EN 61340-3-1

NORME EUROPÉENNE

EUROPÄISCHE NORM

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English version

Electrostatics
Part 3-1: Methods for simulation of electrostatic effects -
Human body model (HBM) -
Component testing
(IEC 61340-3-1:2002)

Electrostatique
Partie 3-1: Méthodes pour la simulation
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CENELEC

European Committee for Electrotechnical Standardization
Comité Européen de Normalisation Electrotechnique
Europäisches Komitee für Elektrotechnische Normung

Central Secretariat: rue de Stassart 35, B - 1050 Brussels

Foreword

The text of document 101/131/FDIS, future edition 1 of IEC 61340-3-1, prepared by IEC TC 101, Electrostatics, was submitted to the IEC-CENELEC parallel vote and was approved by CENELEC as EN 61340-3-1 on 2002-05-01.

The following dates were fixed:

- latest date by which the EN has to be implemented at national level by publication of an identical national standard or by endorsement (dop) 2003-02-01
- latest date by which the national standards conflicting with the EN have to be withdrawn (dow) 2005-05-01

Endorsement notice

The text of the International Standard IEC 61340-3-1:2002 was approved by CENELEC as a European Standard without any modification.

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Electrostatique –

Partie 3-1:

**Méthodes pour la simulation
des effets électrostatiques –**

**Modèle du corps humain (HBM) –
Essais des composants**

Electrostatics –

Part 3-1:

**Methods for simulation of
electrostatic effects –**

**Human body model (HBM) –
Component testing**

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INTERNATIONAL ELECTROTECHNICAL COMMISSION

ELECTROSTATICS –

Part 3-1: Methods for simulation of electrostatic effects –
Human body model (HBM) – Component testing

FOREWORD

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International Standard IEC 61340-3-1 has been prepared by IEC technical committee 101: Electrostatics.

The text of this standard is based on the following documents:

FDIS	Report on voting
101/131/FDIS	101/136/RVD

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 3.

The committee has decided that the contents of this publication will remain unchanged until 2007. At this date, the publication will be

- reconfirmed;
- withdrawn;
- replaced by a revised edition, or
- amended.

INTRODUCTION

Electrostatic discharges occur frequently in the environment. Electrical and electronic equivalent models are used to simulate electrostatic discharges in a controlled manner to allow study and prediction of hazards or damage. One of the most important and widely recognized electrostatic events is the transient current discharge pulse from a human body finger-tip through a grounded object. This type of discharge model is appropriately called the human body model (HBM). This standard provides a description of the modern version of the HBM.

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ELECTROSTATICS –

Part 3-1: Methods for simulation of electrostatic effects – Human body model (HBM) – Component testing

1 Scope

This part of IEC 61340 describes the discharge current waveforms used to define the HBM and the basic equipment requirements used to develop these waveforms. Test parameters are defined for testing and classifying the electrostatic discharge (ESD) sensitivity of non-powered devices to the HBM.

The purpose of this standard is to establish a test model that will replicate HBM failures and will define the HBM transient current discharge waveform and all necessary test parameters to ensure reliable, reproducible test results. Reproducible data will allow accurate comparisons of HBM ESD sensitivity levels.

2 Definitions

For the purpose of this part of IEC 61340, the following definitions apply.

2.1

component

part such as resistor, diode, transistor, integrated circuit or hybrid circuit

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2.2

component failure

condition in which a component does not meet one or more specified static or dynamic data sheet parameters

2.3

component fail window

component fails in a low voltage range but passes at a higher stress level

NOTE For example, a component may fail at 500 V but passes at 1 000 V.

2.4

data sheet parameters

static and dynamic component performance data supplied by the component manufacturer or user

2.5

ESD withstand voltage

maximum ESD level that does not cause component failure

3 Equipment

3.1 HBM ESD waveform generator

This equipment applies a HBM electrostatic current discharge pulse to a component under test. The equivalent circuit and tester evaluation loads are illustrated in figure 1.

3.2 Waveform verification equipment

Equipment capable of verifying the HBM current waveform is defined in this standard. This equipment includes but is not limited to a waveform recording system, a high voltage resistor and a current transducer.

3.2.1 Waveform recording system

The waveform recording system shall have a minimum single shot bandwidth of 350 MHz.

3.2.2 Evaluation loads

Two evaluation loads are necessary to verify the functionality of the waveform generator:

- a) load 1: a shorting wire;
- b) load 2: a $500 \Omega \pm 1 \%$, 1 000 V, low inductance resistor.

The lead length of the evaluation loads (shorting wire or resistor) shall be as short as possible consistent with connecting the evaluation load to the appropriate reference pins (A and B in figure 1) or to any other pins while passing through the current transducer.

3.2.3 Current transducer

The current transducer shall have a minimum bandwidth of 350 MHz.

4 HBM current waveform requirements

4.1 General

For electronic component testing, HBM ESD waveform generator qualification shall ensure waveform integrity of the discharge current through both a shorting wire and a resistive load. The shorting wire waveform requirements are specified in figures 2a and 2b for all positive and negative voltages defined in table 1, while the resistive load waveform requirements for $\pm 1\ 000\text{ V}$ are shown in figure 3 and table 1.

4.2 Waveform qualification and verification

Equipment qualification shall be performed during initial acceptance testing. Re-qualification is required whenever equipment repairs are made that may affect the waveform. Additionally, the waveforms shall be verified periodically. The highest pin count test fixture board should be used. In case the waveform no longer meets the limits in table 1 and figures 2a, 2b and 3, all ESD testing performed after the previous satisfactory waveform check shall be considered invalid.