SLOVENSKI STANDARD

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Semiconductor devices - Mechanical and climatic test methods - Part 4: Damp heat, steady state, highly accelerated stress test (HAST) (IEC 60749- 4:2002)

ICS 31.080.01

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English version

Semiconductor devices –
Mechanical and climatic test methods
Part 4: Damp heat, steady state, highly accelerated stress test (HAST)
(IEC 60749-4:2002)

Dispositifs à semiconducteurs –
Méthodes d'essais mécaniques
et climatiques
Partie 4: Essai continu fortement acceléré
de contrainte de chaleur humide (HAST)
(CEI 60749-4:2002)

Halbleiterbauelemente -
Mechanische und klimatische
Prüfverfahren
Teil 4: Feuchte Wärme, konstant, Prüfung
mit hochbeschleunigter Wirkung (HAST)
(IEC 60749-4:2002)

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CENELEC
European Committee for Electrotechnical Standardization
Comité Européen de Normalisation Electrotechnique
Europäisches Komitee für Elektrotechnische Normung

Central Secretariat: rue de Stassart 35, B - 1050 Brussels

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Foreword

The text of document 47/1602/FDIS, future edition 1 of IEC 60749-4, prepared by IEC TC 47, Semiconductor devices, was submitted to the IEC-CENELEC parallel vote and was approved by CENELEC as EN 60749-4 on 2002-07-02.

This mechanical and climatic test method, as it relates to damp heat, steady state, highly accelerated stress test (HAS), is a complete rewrite of the test contained in clause 4C, chapter 3 of EN 60749:1999.

The following dates were fixed:

– latest date by which the EN has to be implemented at national level by publication of an identical national standard or by endorsement	(dop)	2003-04-01
– latest date by which the national standards conflicting with the EN have to be withdrawn	(dow)	2005-07-01

Endorsement notice

The text of the International Standard IEC 60749-4:2002 was approved by CENELEC as a European Standard without any modification.

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Dispositifs à semiconducteurs –
Méthodes d'essais mécaniques et climatiques –

Partie 4:
Essai continu fortement accéléré de contrainte de chaleur humide (HAST)

Semiconductor devices –
Mechanical and climatic test methods –

Part 4:
Damp heat, steady state, highly accelerated stress test (HAST)

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SEMICONDUCTOR DEVICES – MECHANICAL AND CLIMATIC TEST METHODS –

Part 4: Damp heat, steady state, highly accelerated stress test (HAST)

FOREWORD

1) The IEC (International Electrotechnical Commission) is a worldwide organization for standardization comprising all national electrotechnical committees (IEC National Committees). The object of the IEC is to promote international co-operation on all questions concerning standardization in the electrical and electronic fields. To this end and in addition to other activities, the IEC publishes International Standards. Their preparation is entrusted to technical committees; any IEC National Committee interested in the subject dealt with may participate in this preparatory work. International, governmental and non-governmental organizations liaising with the IEC also participate in this preparation. The IEC collaborates closely with the International Organization for Standardization (ISO) in accordance with conditions determined by agreement between the two organizations.
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International Standard IEC 60749-4 has been prepared by IEC technical committee 47: Semiconductor devices.

The text of this standard is based on the following documents:

FDIS	Report on voting
47/1602/FDIS	47/1618/RVD

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

This mechanical and climatic test method, as it relates to damp heat, steady state, highly accelerated stress test (HAST), is a complete rewrite of the test contained in clause 4C, chapter 3 of IEC 60749.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 3.

The committee has decided that the contents of this publication will remain unchanged until 2007. At this date, the publication will be

- reconfirmed;
- withdrawn;
- replaced by a revised edition, or
- amended.

The contents of the corrigendum of August 2003 have been included in this copy.

SEMICONDUCTOR DEVICES – MECHANICAL AND CLIMATIC TEST METHODS –

Part 4: Damp heat, steady state, highly accelerated stress test (HAST)

1 Scope

This part of IEC 60749 provides a highly accelerated temperature and humidity stress test (HAST) for the purpose of evaluating the reliability of non-hermetic packaged semiconductor devices in humid environments.

2 HAST test – General remarks

The HAST test employs severe conditions of temperature, humidity and bias which accelerate the penetration of moisture through the external protective material (encapsulant or seal) or along the interface between the external protective material and the metallic conductors which pass through it. The stress usually activates the same failure mechanisms as the "85/85" damp heat, steady state humidity test (see IEC 60749-5). As such the test method may be selected from 85 °C/85 % RH steady-state life or from this test method. When both test methods are performed, test results of 85 °C/85 % RH steady-state life take priority over HAST.

This test method shall be considered destructive.

3 Test apparatus

The test requires a pressure chamber capable of maintaining a specified temperature and relative humidity continuously, while providing electrical connections to the devices under test in a specified biasing configuration.

3.1 Controlled conditions

The chamber shall be capable of providing controlled conditions of pressure, temperature and relative humidity during ramp-up to and ramp-down from the specified test conditions.

3.2 Temperature profile

A permanent record of the temperature profile for each test cycle is recommended so that the validity of the stress can be verified.

3.3 Devices under stress

Devices under stress shall be mounted in such a way that temperature gradients are minimized. Devices under stress shall be no closer than 3 cm from internal chamber surfaces, and shall not be subjected to direct radiant heat from heaters. Boards on which devices are mounted should be oriented to minimize interference with vapour circulation.

3.4 Minimize release of contamination

Care shall be exercised in the choice of board and socket materials, to minimize release of contamination and to minimize degradation due to corrosion and other mechanisms.

3.5 Ionic contamination

Ionic contamination of the test apparatus (card cage, test boards, sockets, wiring storage containers, etc.) shall be controlled to avoid test artifacts.

3.6 De-ionized water

De-ionized water with a minimum resistivity of 1×10^4 Ωm at room temperature shall be used.

4 Test conditions

Test conditions consist of a temperature, relative humidity, and duration in conjunction with an electrical bias configuration specific to the device.

4.1 Typical temperature, relative humidity and duration

Table 1 – Temperature, relative humidity and duration requirements

Temperature[a] **(dry bulb)** °C	**Relative humidity**[a] %	**Temperature**[b] **(wet bulb)** °C	**Vapour pressure**[b] kPa	**Duration**[c] h
130 ± 2	85 ± 5	124,7	230	$96\ (^{+2}_{\ 0})$
110 ± 2	85 ± 5	105,2	122	$264\ (^{+2}_{\ 0})$

NOTE 1 For parts that reach absorption equilibrium in 24 h or less, the HAST test is equivalent to at least 1 000 h at 85 °C/85 % RH. For parts that require more than 24 h to reach equilibrium at the specified HAST condition, the time should be extended to allow parts to reach equilibrium.

NOTE 2 Caution: For plastic-encapsulated micro-circuits, it is known that moisture reduces the effective glass transition temperature of the molding compound. Stress temperatures above the effective glass transition temperature may lead to failure mechanisms unrelated to standard 85 °C/85 % RH stress.

[a] Tolerances apply to the entire useable test area.

[b] For information only.

[c] The test conditions are to be applied continuously except during any interim readouts when devices should be returned to stress within the time specified in 5.5. The 96 h and 264 h test durations were selected to be at least equivalent 1 000 h of 85 °C/85 % RH stress using a worst case activation energy of E_a = 0,65 eV.

4.2 Biasing guidelines

Apply bias according to the following guidelines:

a) Minimize power dissipation.

b) Alternate pin bias as much as possible.

c) Distribute potential differences across chip metallization as much as possible.

d) Maximize voltage within operating range.

NOTE The priority of the above guidelines depends on mechanism and specific device characteristics.

e) Either of two kinds of bias can be used to satisfy these guidelines, whichever is more severe:

1) Continuous bias

The d.c. bias shall be applied continuously. Continuous bias is more severe than cycled bias when the die temperature is ≤10 °C higher than the chamber ambient temperature or, if the die temperature is not known when the heat dissipation of the DUT is less than 200 mW. If the heat dissipation of the DUT exceeds 200 mW, then the die temperature should be calculated. If the die temperature exceeds the chamber ambient temperature by more than 5 °C, then the die temperature rise above the chamber ambient should be included in reports of test results since acceleration of failure mechanisms will be affected.

2) Cycled bias

The d.c. voltage applied to the devices under test shall be periodically interrupted with an appropriate frequency and duty cycle. If the biasing configuration results in a temperature rise above the chamber ambient, ΔT_{ja}, exceeding 10 °C, then cycled bias, when optimized for a specific device type, will be more severe than continuous bias. Heating as a result of power dissipation tends to drive moisture away from the die and thereby hinders moisture related failure mechanisms. Cycled bias permits moisture collection on the die during the off periods when device power dissipation does not occur. Cycling the DUT bias with a 50 % duty cycle is optimal for most plastic encapsulated microcircuits. The period of the cycled stress should be ≤2 h for packages ≥2 mm in thickness and ≤30 min for packages <2 mm in thickness. The die temperature, as calculated on the basis of the known thermal impedance and dissipation should be quoted with the results whenever it exceeds the chamber ambient by 5 °C or more.

4.3 Choosing and reporting

Criteria for choosing continuous or cyclical bias, and whether or not to report the amount by which the die temperature exceeds the chamber ambient temperature, are summarized in table 2.

Table 2 – Bias and reporting requirements

ΔT_{ja}	Cyclical bias	Report ΔT_{ja}
ΔT_{ja} < 5 °C, or power per DUT <200 mW	No	No
(ΔT_{ja} ≥ 5 °C or power per DUT ≥200 mW), and ΔT_{ja} < 10 °C	No	Yes
ΔT_{ja} ≥ 10 °C	Yes	Yes