Designation: F 1809 – 97

Standard Guide for Selection and Use of Etching Solutions to Delineate Structural Defects in Silicon [1]

This standard is issued under the fixed designation F 1809; the number immediately following the designation indicates the year of original adoption or, in the case of revision, the year of last revision. A number in parentheses indicates the year of last reapproval. A superscript epsilon (ε) indicates an editorial change since the last revision or reapproval.

1. Scope

1.1 This guide covers the formulation, selection, and use of chemical solutions developed to reveal structural defects in silicon wafers. Etching solutions identify crystal defects that adversely affect the circuit performance and yield of silicon devices. Sample preparation, temperature control, etching technique, and choice of etchant are all key factors in the successful use of an etching method. This guide provides information for several etching solution and allows the user to select according to the need. For further information see Appendix X1and Figs. 1-32 . For a test method for counting preferentially etched or decorated surface defects in silicon wafers see Test Method F 1810.

1.2 *This standard does not purport to address all of the safety concerns, if any, associated with its use. It is the responsibility of the user of this standard to establish appropriate safety and health practices and determine the applicability of regulatory limitations prior to use.*

2. Referenced Documents

2.1 *ASTM Standards:*

D 5127 Practice for Electronic Grade Water [2]

F 1725 Guide for Analysis of Crystallographic Perfection in Silicon Ingots [3]

F 1726 Guide for Analysis of Crystallographic Perfection in Silicon Wafers [3]

F 1727 Practice for Detection of Oxidation Induced Defects in Polished Silicon Wagers [3]

F 1810 Method for Counting Preferentially Etched or Decorated Surface Defects in Silicon Wafers [3]

2.2 *SEMI Specifications:*

SEMI C-1 Specification for Reagents [4]

3. Significance and Use

3.1 Structural defects formed in the bulk of a silicon wafer during its growth or induced by electronic device processing can affect the performance of the circuitry fabricated on that wafer. These defects take the form of dislocations, slip, stacking faults, shallow pits, or precipitates.

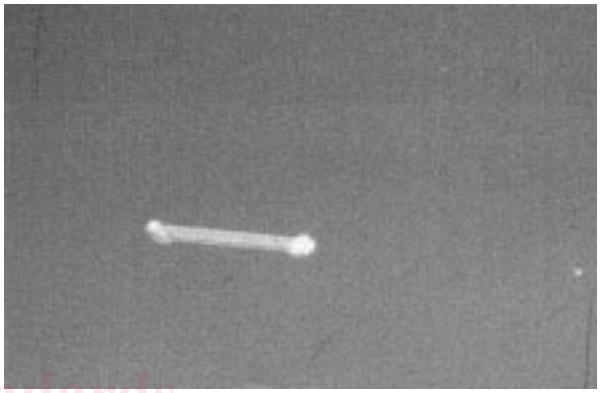

FIG. 1 Secco Etch With Agitation, Oxidation Stacking Fault, 1000x, [100], (1100°C Steam, 80 minutes), ~4 µm removal.

3.2 The exposure of the various defects found on or in a silicon wafer is often the first critical step in evaluating wafer quality or initiating failure analysis of an errant device structure. Etching often accomplishes this task.

4. Interferences

4.1 Complicating factors are different for each etchant. Research the choice of etchants in advance to ensure the

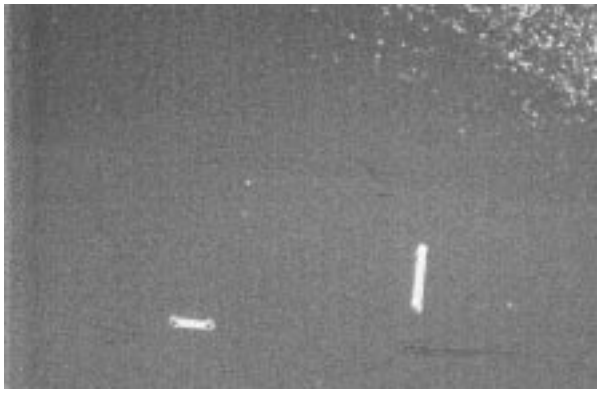

FIG. 2 Secco Etch With Agitation, Oxidation Stacking Fault, 400x, [100], (1100°C Steam, 80 minutes), ~4 µm removal.

[1] This guide is under the jurisdiction of ASTM Committee F01 on Electronics and is the direct responsibility of Subcommittee F01.06 on Silicon Materials and Process Control.

Current edition approved June 10, 1997. Published August 1997.

[2] *Annual Book of ASTM Standards*, 11.01

[3] *Annual Book of ASTM Standards*, Vol 10.05.

[4] Available from Semiconductor Equipment and Materials International, 805 E. Middlefield Rd., Mountain View, CA 94043.

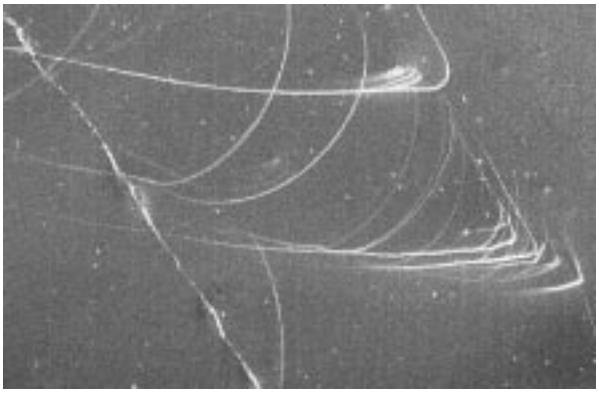

FIG. 3 Secco Etch Without Agitation, Flow Pattern Defect 200x, [100], ~8 µm removal.

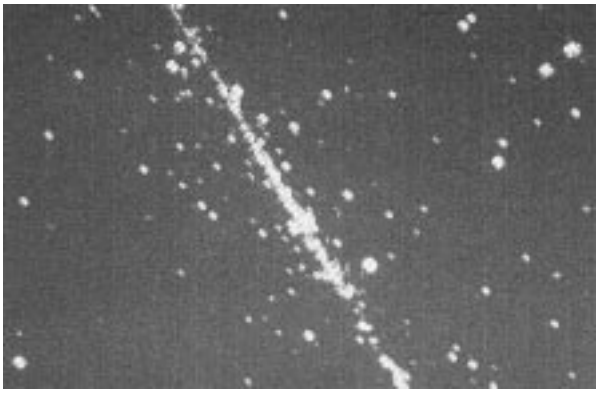

FIG. 6 Secco Etch With Agitation, Scratch Induced Oxidation Stacking Faults, 100x, [100], (1100°C Steam, 80 minutes), ~15 µm removal.

FIG. 4 Secco Etch With Agitation, Expitaxial Stacking Fault, 150x, [100], ~4 µm removal.

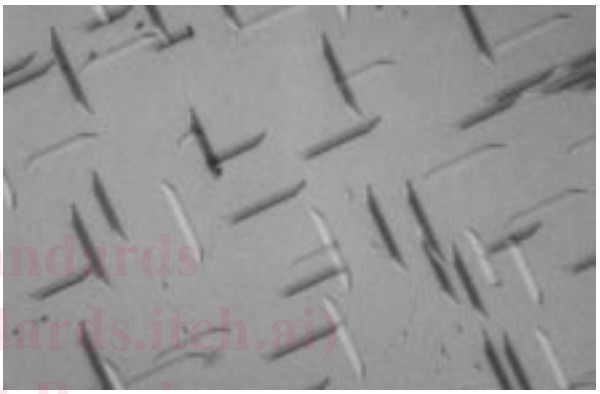

FIG. 7 Wright Etch With Agitation, Damaged Induced Oxidation Stacking Fault, 1000x, [100], (1100°C Steam, 80 minutes).

FIG. 5 Secco Etch With Agitation, Bulk Oxidation Stacking Fault, 200x, [100], (1100°C Steam, 80 minutes), ~15 µm removal.

FIG. 8 Wright Etch With Agitation, Bulk Oxidation Stacking Fault, 500x, [100], (1100°C Steam, 80 minutes).

method and solution are compatible with the sample and objectives. Commonly encountered problems are:

4.1.1 Inadvertent etching through the denuded zone of an oxidized sample delineates irrelevant bulk defects instead of the surface oxidation induced stacking faults (OISF) expected.

4.1.2 Accelerated etching and etching artifacts can result from excessive solution heating during the etching process.

4.1.3 Insufficient agitation, bubble formation or particles in the etching solution can generate artifacts on the silicon surface that mimic actual defects. Insufficient agitation can alter the etching rate, increasing or decreasing it depending upon the formulation.

4.1.4 Any solution in which the oxidation rate is greater than the oxide dissolution rate may form oxide layers that slow or even quench the etching process. The presence of these oxide layers (especially for *N*+ and *P*+ material) obstructs the interpretation of etched defects. Before evaluation, remove any surface oxides.

4.1.5 The wafer surface becomes rougher with longer etch time. This rougher surface does not prevent evaluation under the microscope, but it greatly reduces the effectiveness of visual inspection under bright light.

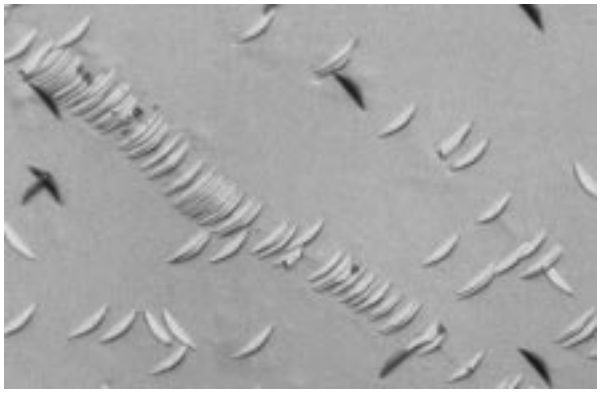

FIG. 9 Wright Etch With Agitation, Scratch Induced Oxidation Stacking Faults, 500x, Boron Doped [100], (1100°C Steam, 80 minutes).

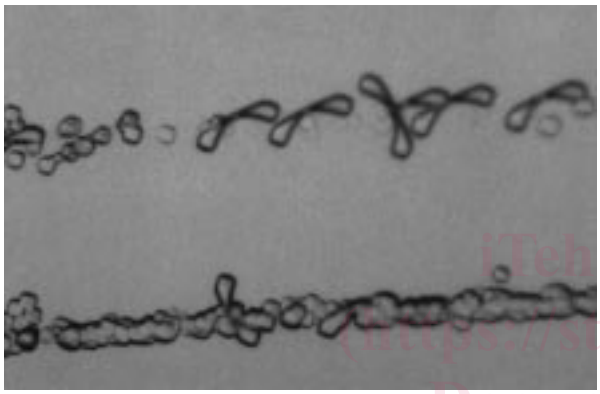

FIG. 10 Wright Etch With Agitation, Scratch Induced Oxidation Stacking Fault, 500x, Antimony Doped, [100], (1100°C Steam, 80 minutes).

FIG. 11 Wright Etch With Agitation, Oxidation Stacking Fault, 500x, Low Resistivity Boron Doped, [100], (1100°C Steam, 80 minutes).

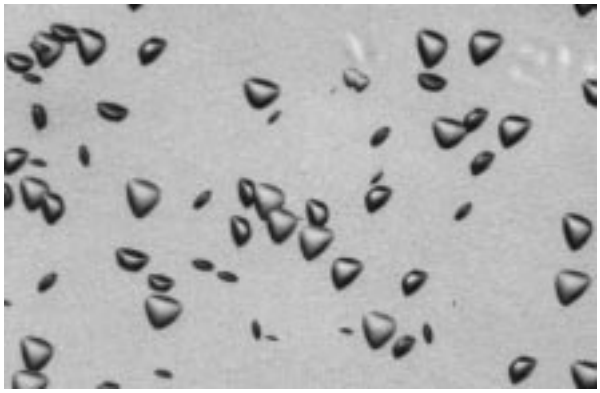

FIG. 12 Wright Etch With Agitation, Oxidation Induced Stacking Faults, 500x, [111], (1100°C Steam, 80 minutes).

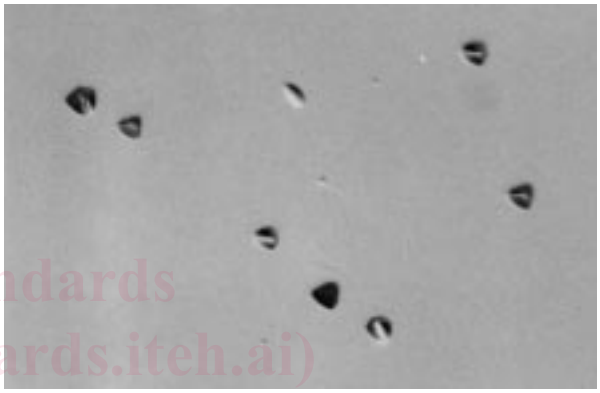

FIG. 13 Wright Etch With Agitation, Slip Dislocations, 500x, [111].

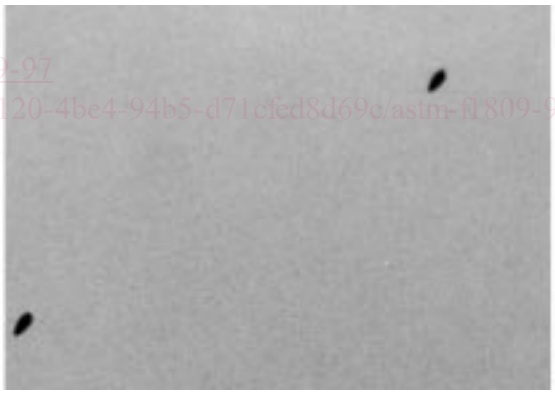

FIG. 14 Wright Etch With Agitation, Slip Dislocations, 200x, [100].

4.1.6 Etching solutions can generate false pits that are not associated with defects.

4.1.7 The samples must be free of work damage, contamination, and other complicating residues. Clean, specular surfaces are suitable for metallographic examination and provide the best results. Surfaces examined should be flat with parallel faces, to simplify microscope inspection.

5. Apparatus

5.1 No standard apparatus or facility satisfies the universal needs for the various etching solutions. Systems range from a simple beaker to large etching tanks complete with nitrogen bubblers, temperature control and nitrous oxide and hydrofluoric acid (HF) scrubbers.

5.1.1 For larger samples (wafers or slugs), use large etching tanks with nitrogen bubble agitation or ultrasonic agitation. Most of the etchant solutions listed work more effectively with the aid of agitation. Heat exchangers or just the thermal mass of the solution can control temperature. Large volumes of acid heat more slowly and allow an intrinsic form of temperature control. To reduce heating effects, maintain 1 L of solution for each 1 000 cm^2 of sample surface area.

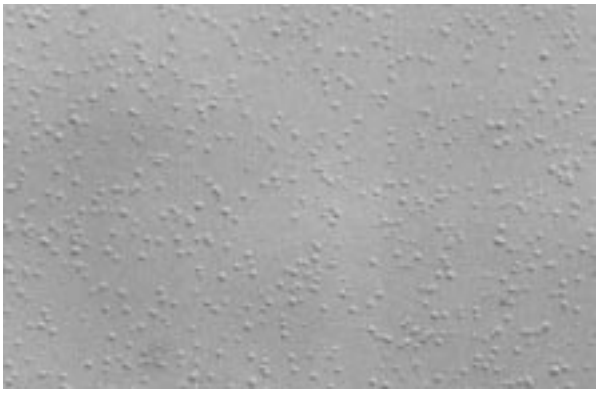

FIG. 15 Wright Etch With Agitation, Shallow Pits (Haze), 500x, Boron Doped [100], (1100°C Steam, 80 minutes).

FIG. 18 Copper-3 Etch With Agitation, Shallow Pits (Haze), 500x, p type, 10 ohm-cm, [111], (1100°C Steam, 80 minutes), 2 µm removal

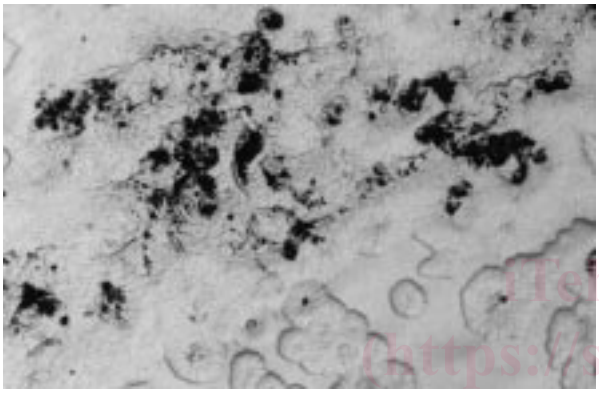

FIG. 16 Wright Etch, Etching Stain-Artifact, 200x, Boron Doped.

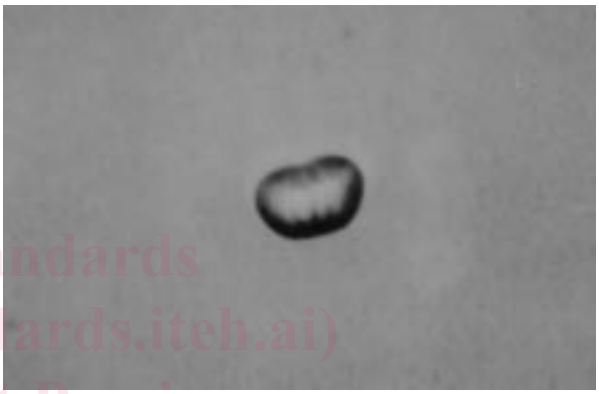

FIG. 19 Copper-3 Etch Without Agitation, Oxidation Stacking Fault, 1000x, p type, 10 ohm-cm, [111], (1100°C Steam, 80 minutes), 1 µm removal.

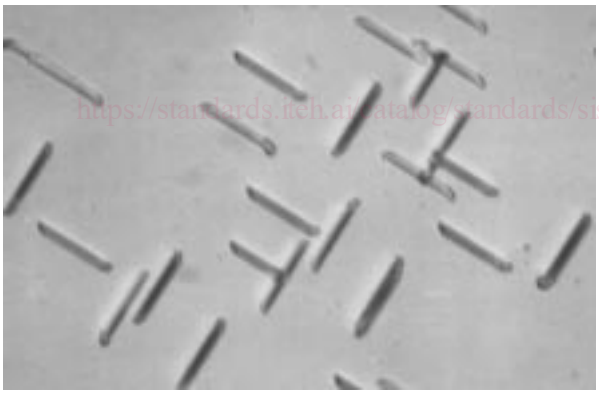

FIG. 17 Copper-3 Etch With Agitation, Oxidation Stacking Fault, 500x, p type, 10 ohm-cm, [100] (1100°C Steam, 80 minutes), 2 µm removal.

FIG. 20 Copper-3 Etch Without Agitation, Oxidation Stacking Fault, 1000x, p type, 10 ohm-cm, [100], (1100°C Steam, 80 minutes), 1 µm removal.

5.1.2 Maintain proper environmental controls. Make provisions to dispose of nitrous oxides, HF fumes, and any solid wastes evolved whatever system is chosen. Chromium and copper-based etching solutions produce solid waste and gaseous byproducts. Chromium-free etching solutions produce no measurable solid waste but do generate nitrous oxides and HF fumes.

6. Reagents and Materials

6.1 All chemicals for which such specifications exist shall conform to SEMI Specification C-1.

6.2 *Purity of Water*—Reference to water means either distilled or deionized water, meeting the requirements of Type I water as defined by Guide D 5127.

6.3 Volume of components describes all solutions in parts of a standard assay. The formulas give solid or dissolved components in grams per 100 mm of total solution.

6.4 All formulations employ a Standard Solution Convention (SSC) that specifies each solution component as an