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Mechanical standardization of semiconductor devices – Part 6: General rules for the preparation of outline drawings of surface mounted semiconductor device packages (IEC 60191-6:2004)

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EUROPEAN STANDARD **EN 60191-6**

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English version

Mechanical standardization of semiconductor devices Part 6: General rules for the preparation of outline drawings of surface mounted semiconductor device packages

(IEC 60191-6:2004)

Normalisation mécanique des dispositifs à semiconducteurs
Partie 6: Règles générales pour la préparation des dessins d'encombrement des dispositifs à semiconducteurs à montage en surface
(CEI 60191-6:2004)

Mechanische Normung von Halbleiterbauelementen
Teil 6: Allgemeine Regeln für die Erstellung von Gehäusezeichnungen von SMD-Halbleitergehäusen
(IEC 60191-6:2004)

This European Standard was approved by CENELEC on 2004-10-01. CENELEC members are bound to comply with the CEN/CENELEC Internal Regulations which stipulate the conditions for giving this European Standard the status of a national standard without any alteration.

Up-to-date lists and bibliographical references concerning such national standards may be obtained on application to the Central Secretariat or to any CENELEC member.

This European Standard exists in three official versions (English, French, German). A version in any other language made by translation under the responsibility of a CENELEC member into its own language and notified to the Central Secretariat has the same status as the official versions.

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CENELEC
European Committee for Electrotechnical Standardization
Comité Européen de Normalisation Electrotechnique
Europäisches Komitee für Elektrotechnische Normung

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Ref. No. EN 60191-6:2004 E

Foreword

The text of document 47D/584/FDIS, future edition 2 of IEC 60191-6, prepared by SC 47D, Mechanical standardization of semiconductor devices, of IEC TC 47, Semiconductor devices, was submitted to the IEC-CENELEC parallel vote and was approved by CENELEC as EN 60191-6 on 2004-10-01.

The following dates were fixed:

– latest date by which the EN has to be implemented at national level by publication of an identical national standard or by endorsement	(dop)	2005-07-01
– latest date by which the national standards conflicting with the EN have to be withdrawn	(dow)	2007-10-01

Annex ZA has been added by CENELEC.

Endorsement notice

The text of the International Standard IEC 60191-6:2004 was approved by CENELEC as a European Standard without any modification.

Annex ZA
(normative)

Normative references to international publications with their corresponding European publications

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

NOTE Where an international publication has been modified by common modifications, indicated by (mod), the relevant EN/HD applies.

Publication	Year	Title	EN/HD	Year
IEC 60191-1	1966	Mechanical standardization of semiconductor devices Part 1: Preparation of drawings of semiconductor devices	-	-
IEC 60191-3	1999	Part 3: General rules for the preparation of outline drawings of integrated circuits	EN 60191-3	1999
IEC 60191-4	1999	Part 4: Coding system and classification into forms of package outlines for semiconductor device packages	EN 60191-4	1999
ISO 1101	1983	Technical drawings - Geometrical tolerancing - Tolerancing of form, orientation, location and run-out - Generalities, definitions, symbols, indications on drawings	-	-

INTERNATIONAL STANDARD

IEC 60191-6

Second edition
2004-09

Mechanical standardization of semiconductor devices –

Part 6: General rules for the preparation of outline drawings of surface mounted semiconductor device packages

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INTERNATIONAL ELECTROTECHNICAL COMMISSION

MECHANICAL STANDARDIZATION OF SEMICONDUCTOR DEVICES –

Part 6: General rules for the preparation of outline drawings of surface mounted semiconductor device packages

FOREWORD

1) The International Electrotechnical Commission (IEC) is a worldwide organization for standardization comprising all national electrotechnical committees (IEC National Committees). The object of IEC is to promote international co-operation on all questions concerning standardization in the electrical and electronic fields. To this end and in addition to other activities, IEC publishes International Standards, Technical Specifications, Technical Reports, Publicly Available Specifications (PAS) and Guides (hereafter referred to as "IEC Publication(s)"). Their preparation is entrusted to technical committees; any IEC National Committee interested in the subject dealt with may participate in this preparatory work. International, governmental and non-governmental organizations liaising with the IEC also participate in this preparation. IEC collaborates closely with the International Organization for Standardization (ISO) in accordance with conditions determined by agreement between the two organizations.

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International Standard IEC 60191-6 has been prepared by subcommittee 47D: Mechanical standardization of semiconductor devices, of IEC technical committee 47: Semiconductor devices.

This second edition of IEC 60191-6 cancels and replaces the first edition, published in 1990 and its amendment 1 (1999), and constitutes a technical revision. This includes the following significant changes with respect to the previous edition: improvement of the geometrical drawing format and addition of the examples of the drawing of major packages.

The text of this standard is based on the following documents:

FDIS	Report on voting
47D/584/FDIS	47D/587/RVD

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

The committee has decided that the contents of this publication will remain unchanged until the maintenance result date indicated on the IEC web site under "http://webstore.iec.ch" in the data related to the specific publication. At this date, the publication will be

- reconfirmed;
- withdrawn;
- replaced by a revised edition, or
- amended.

A bilingual version of this publication may be issued at a later date.

MECHANICAL STANDARDIZATION OF SEMICONDUCTOR DEVICES –

Part 6: General rules for the preparation of outline drawings of surface mounted semiconductor device packages

1 Scope

This part of IEC 60191 gives general rules for the preparation of outlines drawings of surface-mounted semiconductor devices. It supplements IEC 60191-1 and 60191-3. It covers all surface-mounted devices-discrete semiconductors as well as integrated circuits classified as form E in Clause 3 of IEC 60191-4.

2 Normative references

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60191-1:1966, *Mechanical standardization of semiconductor devices – Part 1: Preparation of drawings of semiconductor devices*

IEC 60191-3:1999, *Mechanical standardization of semiconductor devices – Part 3: General rules for the preparation of outline drawings of integrated circuits*

IEC 60191-4:1999, *Mechanical standardization of semiconductor devices – Part 4: Coding system and classification into forms of package outlines for semiconductor devices*

ISO 1101:1983, *Technical drawings – Geometrical tolerancing – Tolerancing of form, orientation, location and run-out – Generalities, definitions, symbols, indications on drawings*

3 Definitions

For the purposes of this document, the following definitions apply.

3.1
seating plane
plane which designates the plane of contact of the package, including any stand-off, with the surface on which it will be mounted

NOTE This plane is often used as the reference plane.

3.2
reference plane
plane parallel to the seating plane at a distance A3 above seating plane (does not apply to leadless package)

The distance A3 is known as the reference plane distance. It determines the terminal projection zone (see Figure 1).

NOTE This distance is a theoretical dimension which is not related to any feature of the package. Its value is chosen for each package so the length of terminal projection zone L_p is a good approximation of the terminal length used for mounting, e.g. the length of the part of the terminal that is soldered to the substrate.

3.3
terminal position area
maximum area on the seating plane within which the terminal projection zone is located, taking into account the maximum values of L_p and b_p

The surface of the terminal position area is equal to $l_1 \times b_3$ with, generally

$$l_1 = L_p \text{ max.} + (\text{HDmax} - \text{HDmin})/2$$

$$= L_p \text{ max.} + (\text{HEmax} - \text{HEmin})/2$$

$$\text{and } b_3 = b_p \text{ max.} + x$$

Checking can be carried out by means of an appropriate gauge (see Figure 2).

3.4
pattern of terminal position areas
group of all terminal position areas of a leaded package or folded lead package in the seating plane

For a leadless package, it is the projection of its metallized pads or terminals on the seating plane.

The true positions of the centres of the terminal position areas are located on a grid with as modulus

$$e / e_D \quad \text{or} \quad e / e_E$$

The pattern of terminal position areas does not include tolerances stemming from mounting substrates (printed board) design and placement machine accuracy.

3.5
coplanarity of terminals
the requirement for coplanarity of terminals is given in a tolerance frame showing the ISO symbol for profile of a surface, the tolerance value *y* and the reference to the seating plane

Where the part of the terminal intended for soldering is a flat zone of defined dimension $b \times l$, with nominal position on the seating plane – e.g. pads of leadless packages – then the requirement for coplanarity of terminals is strictly the ISO requirement for flatness applied to these zones.

In all the other cases, the requirement for coplanarity of terminals is clarified by note.

3.6
datum
theoretically, the exact geometrical reference is established for controlling the tolerance zone when specifying a geometrical tolerance as a related feature

NOTE Datum S should be established by seating plane.

4 Design rules

The outline drawing of a surface-mounted semiconductor device package shall comprise in the given sequence

– the drawing (strictly speaking);
– the tables of dimensions;
– the notes to the tables and the drawings;
– the indication of supporting countries;
– the codification.

The drawing shall conform with the general rules for drawings laid down in IEC 60191-1 sections 1 and 2, as well as with the specific definitions of Clause 3 above.

The following Clauses 5 and 6 give, respectively, the tables of dimensions to be specified and the notes to be called, where relevant. Supplementary dimensions and notes may be added when required.

The codification of package outlines shall be in accordance with IEC 60191-4.

5 Dimensions to be specified

Crosses in Tables 1 and 2 indicate where values have to be specified. In the auxiliary right-hand column, a code indicates for which outline families each dimension is generally relevant, as follows:

L:	leaded packages	packages with gull-wing leads	for example; QFP, SOP,TSOP
F:	folded lead packages	packages with J-bent leads	for example; QFJ, SOJ
P:	leadless packages	packages with no leads	for example; QFN
B:	ball grid array packages	packages with ball leads	for example; BGA

6 Notes

Notes referred to in the tables and in the drawings appear after Table 2; in the auxiliary right-hand column, a code indicates for which outline families each note is generally relevant (with the same code as in Clause 5).

For each particular outline package or package family, the applicable notes shall be numbered sequentially from 1 in the order in the tables and then on the drawing.