
**Standardizacija mehanskih lastnosti polprevodniških elementov – 6-12. del:
Splošna pravila za pripravo tehničnih risb okrovov polprevodniških elementov za
površinsko montažo - Vodilo za konstruiranje drobne rasterske mreže priključkov
v ravnini (FLGA) – Pravokotni tip (IEC 60191-6-12:2002)**

Mechanical standardization of semiconductor devices -- Part 6-12: General rules for the preparation of outline drawings of surface mounted semiconductor device packages - Design guide for fine-pitch land grid array (FLGA) - Rectangular type

Mechanische Normung von Halbleiterbauelementen -- Teil 6-12: Allgemeine Regeln für die Erstellung von Gehäusezeichnungen von SMD-Halbleitergehäusen - Konstruktionsleitfaden für Feinraster-Land-Grid-Array (FLGA) - Rechteckige Ausführung

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Normalisation mécanique des dispositifs à semiconducteurs -- Partie 6-12: Règles générales pour la préparation des dessins d'encombrement des dispositifs à semiconducteurs pour montage en surface - Guide de conception pour les boîtiers FLGA de type rectangulaire

Ta slovenski standard je istoveten z: EN 60191-6-12:2002

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EUROPEAN STANDARD

EN 60191-6-12

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English version

Mechanical standardization of semiconductor devices
Part 6-12: General rules for the preparation of outline drawings
of surface mounted semiconductor device packages -
Design guide for fine-pitch land grid array (FLGA) -
Rectangular type
(IEC 60191-6-12:2002)

Normalisation mécanique
 des dispositifs à semiconducteurs
 Partie 6-12: Règles générales pour la
 préparation des dessins d'encombrement
 des dispositifs à semiconducteurs
 pour montage en surface -
 Guide de conception pour les boîtiers
 FLGA de type rectangulaire
 (CEI 60191-6-12:2002)

Mechanische Normung
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 Erstellung von Gehäusezeichnungen
 von SMD-Halbleitergehäusen -
 Konstruktionsleitfaden für Feinraster-
 Land-Grid-Array (FLGA) -
 Rechteckige Ausführung
 (IEC 60191-6-12:2002)

This European Standard was approved by CENELEC on 2002-07-01. CENELEC members are bound to comply with the CEN/CENELEC Internal Regulations which stipulate the conditions for giving this European Standard the status of a national standard without any alteration.

Up-to-date lists and bibliographical references concerning such national standards may be obtained on application to the Central Secretariat or to any CENELEC member.

This European Standard exists in three official versions (English, French, German). A version in any other language made by translation under the responsibility of a CENELEC member into its own language and notified to the Central Secretariat has the same status as the official versions.

CENELEC members are the national electrotechnical committees of Austria, Belgium, Czech Republic, Denmark, Finland, France, Germany, Greece, Hungary, Iceland, Ireland, Italy, Luxembourg, Malta, Netherlands, Norway, Portugal, Slovakia, Spain, Sweden, Switzerland and United Kingdom.

CENELEC

European Committee for Electrotechnical Standardization
 Comité Européen de Normalisation Electrotechnique
 Europäisches Komitee für Elektrotechnische Normung

Central Secretariat: rue de Stassart 35, B - 1050 Brussels

Foreword

The text of document 47D/493/FDIS, future edition 1 of IEC 60191-6-12, prepared by SC 47D, Mechanical standardization of semiconductor devices, of IEC TC 47, Semiconductor devices, was submitted to the IEC-CENELEC parallel vote and was approved by CENELEC as EN 60191-6-12 on 2002-07-01.

The following dates were fixed:

- latest date by which the EN has to be implemented at national level by publication of an identical national standard or by endorsement (dop) 2003-04-01
- latest date by which the national standards conflicting with the EN have to be withdrawn (dow) 2005-07-01

Annexes designated "normative" are part of the body of the standard.
In this standard, annex ZA is normative.
Annex ZA has been added by CENELEC.

Endorsement notice

The text of the International Standard IEC 60191-6-12:2002 was approved by CENELEC as a European Standard without any modification.

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Annex ZA (normative)

Normative references to international publications with their corresponding European publications

This European Standard incorporates by dated or undated reference, provisions from other publications. These normative references are cited at the appropriate places in the text and the publications are listed hereafter. For dated references, subsequent amendments to or revisions of any of these publications apply to this European Standard only when incorporated in it by amendment or revision. For undated references the latest edition of the publication referred to applies (including amendments).

NOTE When an international publication has been modified by common modifications, indicated by (mod), the relevant EN/HD applies.

<u>Publication</u>	<u>Year</u>	<u>Title</u>	<u>EN/HD</u>	<u>Year</u>
IEC 60191	Series	Mechanical standardization of semiconductor devices	EN 60191	Series

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INTERNATIONAL STANDARD

IEC 60191-6-12

First edition
2002-06

**Mechanical standardization of semiconductor devices –
Part 6-12:
General rules for the preparation of outline drawings
of surface mounted semiconductor device packages –
Design guide for fine-pitch land grid array (FLGA) –
Rectangular type**

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Partie 6-12:

*Règles générales pour la préparation des dessins
d'encombrement des dispositifs à semiconducteurs
pour montage en surface –
Guide de conception pour les boîtiers FLGA
de type rectangulaire*

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International Electrotechnical Commission, 3, rue de Varembé, PO Box 131, CH-1211 Geneva 20, Switzerland
Telephone: +41 22 919 02 11 Telefax: +41 22 919 03 00 E-mail: inmail@iec.ch Web: www.iec.ch



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INTERNATIONAL ELECTROTECHNICAL COMMISSION

MECHANICAL STANDARDIZATION OF SEMICONDUCTOR DEVICES –**Part 6-12: General rules for the preparation of outline drawings
of surface mounted semiconductor device packages –
Design guide for fine-pitch land grid array (FLGA) –
Rectangular type**

FOREWORD

- 1) The IEC (International Electrotechnical Commission) is a worldwide organization for standardization comprising all national electrotechnical committees (IEC National Committees). The object of the IEC is to promote international co-operation on all questions concerning standardization in the electrical and electronic fields. To this end and in addition to other activities, the IEC publishes International Standards. Their preparation is entrusted to technical committees; any IEC National Committee interested in the subject dealt with may participate in this preparatory work. International, governmental and non-governmental organizations liaising with the IEC also participate in this preparation. The IEC collaborates closely with the International Organization for Standardization (ISO) in accordance with conditions determined by agreement between the two organizations.
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International Standard IEC 60191-6-12 has been prepared by subcommittee 47D: Mechanical standardization of semiconductor devices, of IEC technical committee 47: Semiconductor devices.

The text of this standard is based on the following documents:

FDIS	Report on voting
47D/493/FDIS	47D/507/RVD

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 3.

A bilingual version of this publication may be issued at a later date.

The committee has decided that the contents of this publication will remain unchanged until 2004. At this date, the publication will be

- reconfirmed;
- withdrawn;
- replaced by a revised edition, or
- amended.

INTRODUCTION

The demand for area array style packages exists because of the multi-functions and high performance of electrical equipment. The objective of this design guide is to standardize outlines and to get interchangeability of FLGA rectangular type packages. The terminal pitch and package outlines of these fine-pitch array packages are smaller than those of LGA packages.

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MECHANICAL STANDARDIZATION OF SEMICONDUCTOR DEVICES –

Part 6-12: General rules for the preparation of outline drawings of surface mounted semiconductor device packages – Design guide for fine-pitch land grid array (FLGA) – Rectangular type

1 Scope

This part of IEC 60191 provides common outline drawings and dimensions for all types of structures and composed materials of fine-pitch land grid array (hereinafter called FLGA) whose terminal pitch is less than, or equal to, 0,80 mm and whose package body outline is rectangular.

2 Normative references

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60191 (all parts), *Mechanical standardization of semiconductor devices*

3 Definitions

For the purposes of this part of IEC 60191, the following definitions, as well as those given in the other parts of this series, apply.

3.1

flanged type

type whose package body size (body length and width) consists of its own flange composed around the encapsulation or lid

3.2

type of real chip size

type whose package body size (body length and width) consists of an encapsulation around the real chip only

3.3

FLGA

packages with metal lands or metal bumps of which the terminal height is less than, or equal to, 100 μm , and whose terminal pitch is less than, or equal to, 0,80 mm, positioned in an array on the base plane of the package as external terminals

This package structure makes it possible to surface-mount the packages to the printed circuit board.

3.4

material designation

FLGA packages are classified according to the following two material designations:

3.4.1

plastic type (P-FLGA)

plastic-type classification is assigned to packages which consist of resin substrate as interposer material (for example, glass-epoxy, poly-imid)

3.4.2

ceramic type (C-FLGA)

ceramic-type classification is assigned to packages which consist of ceramic substrate as interposer material