

**SLOVENSKI STANDARD  
SIST EN 61523-1:2002****01-september-2002**

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**Delay and power calculation standards - Part 1: Integrated circuit delay and power calculation systems (IEC 61523-1:2001)**

Delay and power calculation standards -- Part 1: Integrated circuit delay and power calculation systems

Berechnung von Verzögerung und Leistungsaufnahme beim Entwurf von Chips -- Teil 1: System zur Berechnung von Verzögerung und Leistungsaufnahme integrierter Schaltkreise (IC)

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Normes de calculs de puissance et de temps de retard -- Partie 1: Systèmes de calcul de puissance et de temps de retard des circuits intégrés

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**Delay and power calculation standards**  
**Part 1: Integrated circuit delay and power**  
**calculation systems**  
(IEC 61523-1:2001)

Normes de calculs de puissance  
et de temps de retard  
Partie 1: Systèmes de calcul  
de puissance et de temps  
de retard des circuits intégrés  
(CEI 61523-1:2001)

Berechnung von Verzögerung  
und Leistungsaufnahme beim  
Entwurf von Chips  
Teil 1: System zur Berechnung von  
Verzögerung und Leistungsaufnahme  
integrierter Schaltkreise (IC)  
(IEC 61523-1:2001)

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European Committee for Electrotechnical Standardization  
Comité Européen de Normalisation Electrotechnique  
Europäisches Komitee für Elektrotechnische Normung

**Central Secretariat: rue de Stassart 35, B - 1050 Brussels**

## Foreword

The text of document 93/143/FDIS, future edition 1 of IEC 61523-1, prepared by IEC TC 93, Design automation, was submitted to the IEC-CENELEC parallel vote and was approved by CENELEC as EN 61523-1 on 2001-12-04.

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- latest date by which the EN has to be implemented at national level by publication of an identical national standard or by endorsement (dop) 2002-09-01
- latest date by which the national standards conflicting with the EN have to be withdrawn (dow) 2004-12-01

This standard is based on IEEE Std P1481:1999; IEEE Standard for delay and power calculation systems.

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## Endorsement notice

The text of the International Standard IEC 61523-1:2001 was approved by CENELEC as a European Standard without any modification.

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# INTERNATIONAL STANDARD

# IEC 61523-1

First edition  
2001-09

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## Delay and power calculation standards –

### Part 1: Integrated circuit delay and power calculation systems

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## INTERNATIONAL ELECTROTECHNICAL COMMISSION

**DELAY AND POWER CALCULATION STANDARDS –****Part 1: Integrated circuit delay and power calculation systems**

## FOREWORD

- 1) The IEC (International Electrotechnical Commission) is a worldwide organization for standardization comprising all national electrotechnical committees (IEC National Committees). The object of the IEC is to promote international co-operation on all questions concerning standardization in the electrical and electronic fields. To this end and in addition to other activities, the IEC publishes International Standards. Their preparation is entrusted to technical committees; any IEC National Committee interested in the subject dealt with may participate in this preparatory work. International, governmental and non-governmental organizations liaising with the IEC also participate in this preparation. The IEC collaborates closely with the International Organization for Standardization (ISO) in accordance with conditions determined by agreement between the two organizations.
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International Standard IEC 61523-1 has been prepared by IEC technical committee 93: Design automation.

This standard is based on IEEE Std P1481 (1999): *IEEE Standard for delay and power calculation systems*.

The text of this standard is based on the following documents:

FDIS	Report on voting
93/143/FDIS	93/144/RVD

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

*This standard does not follow the rules for the structure of international standards given in Part 3 of the ISO/IEC Directives.*

IEC 61523 consists of the following parts, under the general title: *Delay and calculation standards*:

IEC 61523-1, Part 1: *Integrated circuit delay and power calculation systems*

IEC 61523-2, Part 2: *Prelayout delay calculation model specification of CMOS ASIC libraries* (to be published)

The committee has decided that the contents of this publication will remain unchanged until 2006. At this date, the publication will be

- reconfirmed;
- withdrawn;
- replaced by a revised edition, or
- amended.

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