# SLOVENSKI STANDARD
# SIST EN 190000:2002

**01-september-2002**

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**Generic specification: Monolitic integrated circuits**

Generic Specification: Monolithic integrated circuits

Fachgrundspezifikation: Monolitische integrierte Schaltungen

Spécification générique: Circuits intégrés monolithiques



**Ta slovenski standard je istoveten z:** **EN 190000:1995**

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**ICS:**

| | | |
|---|---|---|
| 31.200 | Integrirana vezja, mikroelektronika | Integrated circuits. Microelectronics |

**SIST EN 190000:2002** **en**

EUROPEAN STANDARD

NORME EUROPÉENNE

EUROPÄISCHE NORM

# EN 190000

June 1995

Supersedes CECC 90 000:1990

Descriptors: Quality, electronic components, monolithic integrated circuits

English version

## Generic Specification: Monolithic integrated circuits

Spécification générique: Circuits intégrés monolithiques

Fachgrundspezifikation: Monolitische integrierte Schaltungen



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Up-to-date lists and bibliographical references concerning such national standards may be obtained on application to the Central Secretariat or to any CENELEC member.

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CENELEC

European Committee for Electrotechnical Standardization
Comité Européen de Normalisation Electrotechnique
Europäisches Komitee für Elektrotechnische Normung

Central Secretariat: rue de Stassart 35, B - 1050 Brussels



Ref. No. EN 190000:1995 E

## FOREWORD

This European Standard was prepared by Working Group CLC/TC CECC/WG 9 "Integrated Circuits".

The text of the draft based on CECC 90 000:1990 (Issue 4) and documents CECC(Secretariat)2739, 2740, 2741, 2567, 2565, 2570, 2644, 2668, 2669, 2566, 2645, 2646 and 3117 was submitted to the formal vote. Together with the voting reports, circulated as documents CECC(Secretariat)3187, 2632, 2631, 2674, 2784, 2790, 3189, 2726, 2785, 2786 and 3251, it was approved as EN 190000 on 1992-11-28.

This European Standard supersedes CECC 90 000:1990.

The following dates were fixed:

- latest date by which the EN has to be implemented at national level by publication of an identical national standard or by endorsement (dop) 1996-01-11

- latest date by which national standards conflicting with the EN have to be withdrawn (dow) 2004-01-11

# CONTENTS

# 1 SCOPE

This specification specifies the terms, definitions, symbols, test methods and other material for monolithic integrated (micro)circuits (*), as defined in IEC 747, necessary to prepare appropriate detail specifications (DS) in the CECC System. Supplementary requirements for different families of integrated microcircuits are included in separate specifications.

(*) In the following the term "integrated circuits" is used.

# 2 GENERAL

## 2.1 Order of precedence

Where any discrepancies occur for any reason, documents shall rank in the following order of authority :

- the detail specification (DS)
- the sectional specification (SS)
- the generic specification (GS)
- the internal regulation of the FEN e.V.
- any other international documents to which reference is made.

The same order of precedence shall apply to equivalent national documents.

## 2.2 Related documents



In each case the latest issue of the documents prior to the date of issue of this document is valid.



| | |
|---|---|
| ISO 1 000 | SI units and recommendations for the use of their multiples and of certain other units. |
| IEC 27-1 | Letter symbols to be used in electrical technology. General. |
| IEC 50 | International Electrotechnical Vocabulary. |
| IEC 68 | Basic environmental testing procedures. |
| IEC 134 | Rating systems for electronic tubes and valves and analogous semiconductor devices. |
| IEC 148 | Letter symbols for semiconductor devices and integrated microcircuits (Chapter X). |
| IEC 617 | Graphical symbols for diagrams. |
| IEC 617-12 | Part 12 : Binary logic elements. |
| IEC 617-13 | Part 13 : Analogue elements. |
| IEC 747 | Semiconductor devices - Discrete devices and integrated circuits. |
| IEC 747-1 | Part 1 : General. |
| IEC 747-10 | Part 10 : Generic specification for discrete devices and integrated circuits. |
| IEC 748 | Semiconductor devices - Integrated circuits. |

IEC 748-1 Part 1 : General.

IEC 748-2 Part 2 : Digital integrated circuits.

IEC 748-3 Part 3 : Analogue integrated circuits.

IEC 748-4 Part 4 : Interface integrated circuits.

IEC 749 Semiconductor devices : Mechanical and climatic test methods.

IEC 191 Mechanical standardization of semiconductor devices.

CECC 00 007 Basic specification : Sampling plans and procedures for inspection and attributes.

CECC 00 114 Quality Assessment Procedures.

Internal Regulations of the FEN e.V. and CECC Rules of Procedure.

## 2.3 Units, symbols and terminology

### 2.3.1 General

Units, graphical symbols, letter symbols and terminology shall, whenever possible, be taken from the following documents :



ISO 1000 SI units and recommendations for the use of their multiples and of certain other units.

IEC 27 Letter symbols to be used in electrical technology.



IEC 50 International Electrotechnical Vocabulary.

IEC 617 Graphical symbols for diagrams.

Any other units, symbols, and terminology required shall be derived in accordance with the principles of the documents listed above in 2.2.

### 2.3.2 General terms for integrated circuits

| | |
|---|---|
| - Microelectronic | IEC 748-1 chapter IV clause 1.5 |
| - Microcircuit | IEC 748-1 chapter IV clause 2.2 |
| - Integrated circuit | IEC 748-1 chapter IV clause 2.3 |
| - Integrated microcircuit | IEC 748-1 chapter IV clause 2.4 |
| - Microassembly | IEC 748-1 chapter IV clause 2.5 |

## 2.4 Standard and preferred values

Standard and preferred values should preferably be chosen from the relevant IEC Publications :

| | |
|---|---|
| - dimensions | IEC 191-2 |
| - voltages | IEC 747-1 |
| - temperatures | IEC 747-1 |

Preferred values are :

- 65, - 55, - 40, - 25, 0, + 25, + 70, + 85, + 125, + 150 °C.

## 2.5 Marking of component and package

Apart from statutory hazard warnings which shall, if necessary, take first priority, the following shall be marked on the device, in order of precedence, as space permits. All information except the terminal marking, shall also appear on the primary package used as initial protection or wrapping for delivery.

(1) Terminal identification (for example position of pin n° 1), (see 2.5.1)

(2) Type designation (standardized or commercial)

(3) Operating temperature range (if not included in (2), in Pro-electron* code)

(4) Quality assessment level applied (in code) followed by Z in case of devices supplied under Capability Approval

(5) Screening class applied (in code)

(6) Date code (year/week) of the week in which the device is encapsulated encoded into three or four digits as given in standard ISO 2015.

(7) CECC Mark of Conformity

(8) Manufacturer's name or trade mark (may include factory code, see 2.5.2)

(9) Factory identification code (if not included in (8), see 2.5.2)

(10) Package materials (if not included in (2), in Pro-electron* code)

(11) Caution label for Electrostatic Sensitive Devices (see 2.5.3)

(12) Optional tests (in code), (see 2.5.4)



(*) "Pro-electron code" means the suitable parts for temperatures and for materials from the Pro-electron type description code for integrated circuits.

### 2.5.1 Terminal identification

The terminals shall be identified in at least one of the following ways :

- in accordance with the specified outline or basic drawing
- as given in the DS.

### 2.5.2 Factory identification code

An identification code is allocated to each factory of each manufacturer whose Chief Inspector is responsible for certifying components.

The manufacturer is the allocating authority for letters and/or figures indicating the responsible centre. This code shall be published in CECC 00 200 (QPL).

### 2.5.3 Precautions for Electrostatic Sensitive Devices

All integrated circuits covered by this specification are regarded as Electrostatic Sensitive Devices and as such require special packaging and handling precautions to eliminate damage or potential weakening of devices.

Devices shall be packed so that they are protected against electrostatic fields.

### 2.5.4 Optional tests

Sectional specifications (SS) may give the possibility to apply optional test(s). Each test or combination of tests is coded in the following way :

Blank : No optional test

1 Salt mist, see 4.6.14

2 Combination of optional tests of assessment level P applicable to components for use for example in telecommunication equipment.

The following optional tests are applied to components qualified to :

CECC 90 103 : Sub-Groups A3a, D3
CECC 90 104 : Sub-Groups A3a, B4, D3, D4
CECC 90 109 : Sub-Groups A3a, B4, D3, D4



3 à 8 To be included later

9 Special test and/or special tests combinations not called for in the CECC System.



### 2.5.5 Marking symbols location

The marking symbols shall be located in the following order :

Fig. 1 is an example for packages with sufficient space. The bottom side of the package is available for manufacturer's additional marking.

Fig. 2 is an example for small packages. The lower part of the bottom side is available for manufacturer's additional marking.

The marking of cylindrical packages will be included later.

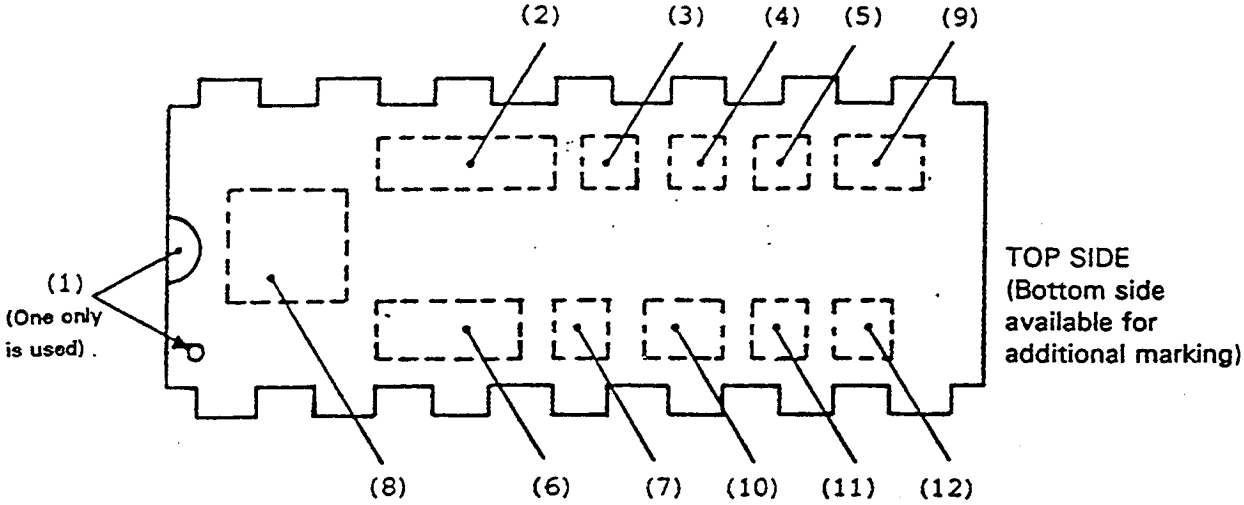


FIGURE 1



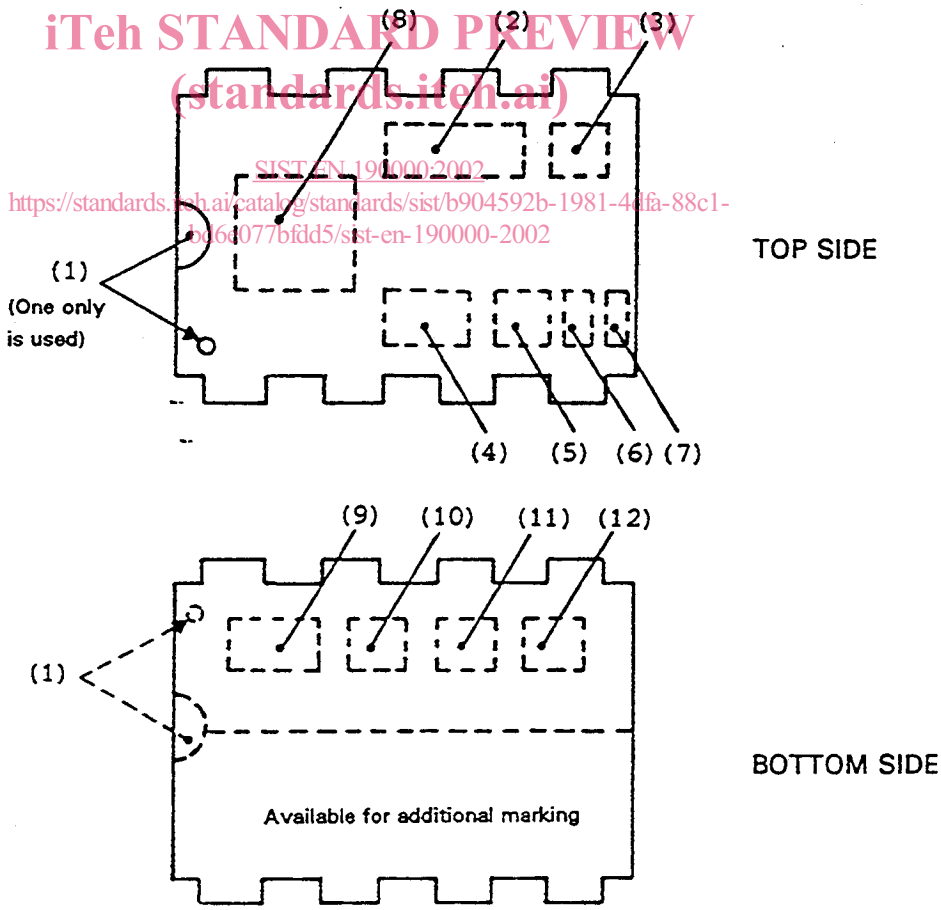


FIGURE 2

## 2.6 Ordering information

The following information shall be included in the order and also in the delivery documents. The package shall include sufficient information to relate to the delivery :

(1) Manufacturer

(2) Standardized or commercial type designation

(3) Operating temperature range (if not included in (2), Pro-electron code may be used)

(4) Required quality assessment level (in code)

(5) Required optional test (salt mist for example), (in code, if applicable)

(6) Required screening class (in code, if applicable)

(7) Package shape (Pro-electron code may be used)

(8) Package materials (Pro-electron code may be used)

(9) Terminals metal and coating (if applicable)

(10) Relevant DS number and, if necessary, issue and date.



Example : wording in the following order :

"N integrated circuits XXXX CD 4011B, C, Y level with optional test 1, B Class, DG package, gold plated kovar terminals to CECC 90 104-XXX, Issue 1 of 198x".



means :

N integrated circuits manufactured by XXXX, type number CD 4011B, operating temperature - 55 °C to + 125 °C, under quality assessment level Y including optional test of salt mist, screened in B class, in glass sealed ceramic "dual in line" package, with gold plated kovar terminals, in compliance with DS CECC 90 104-XXX, Issue 1 of 198x.

# 3 QUALITY ASSESSMENT PROCEDURES

## 3.1 Primary stage of manufacture and subcontracting

The primary stage for bipolar integrated circuits is the first process which changes the monocrystalline semiconductors material from being either wholly P-type or wholly N-type. The primary stage for MOS circuits is the first oxidation of the substrate.

When the approved manufacturer invokes CECC 00 114 for subcontracting, he shall ensure that the following conditions are satisfied :

- when subcontracting is not done in one of his company's factories, the subcontracted manufacturing processes may be either the wafer fabrication or the assembly of the device ;

- the National Supervising Inspectorate (ONS) shall be satisfied that the Chief Inspector of the manufacturer who is certifying the components under the CECC System has the responsibility for inspection of the work and the inspection arragements there ;

- the Chief Inspector shall be provided with the production line process charts, the defined inspection points, the inspection requirements at each stage and the quality control requirements, together with the procedures for the transfer of the parts from the place of manufacture to the manufacturer within the CECC who is certifying the component. The ONS shall be informed and have access to this documentation and be able to verify the application of these requirements ;

- any changes in inspection requirements and manufacturing procedures shall be reported back to the CECC approved manufacturer's Chief Inspector who is certifying the components. The significant changes shall be reported by the approved manufacturer's Chief Inspector to the ONS ;

- the approved manufacturer shall perform the quality conformance inspection tests (Groups A, B, C, D) prescribed by the DS for the component he is certifying. He can perform the Groups A and B tests in a facility outside a CECC member country, provided that this facility is supervised by the ONS. Groups C and D tests shall be performed in one of his company's factories located in a CECC member country.

On the other hand quality conformance inspection tests can be subcontracted to approved test laboratories within the CECC geographical area.

## 3.2 Structural similarity procedures

### 3.2.1 General rules



(1) Purpose

Structural similarity procedures are intended to reduce the amount of testing that shall be performed for quality assessment purposes.



(2) Principles

For a test applicable to a group of device types, the test may be performed on one type from the group and the results obtained are considered as representative for all the types, if the general and particular criteria for structural similarity described in this section and applicable to this test are complied with. The definition of these criteria shall be based on the principle that conformity and reliability verified on the representative type gives at least the same conformity and reliability assurance for the associated types.

Structural similarity shall not be applied for electrical and visual tests under Group A.

(3) Application conditions

Tests and measurements specified in sequence.

Structural similarity procedures apply to a single test.

In a sequence of tests in a Sub-Group, excluding end point tests, the test considered to be most critical shall be used to decide the criteria for structural similarity grouping. Where there are end point tests these shall not be used to decide the structural similarity criteria, e.g. B4 tests, where Sealing or Accelerated Damp Heat are used as part of the end point test sequence for Rapid Change of Temperature.

An example of practical application of structural similarity procedures is given in Annex E of this generic specification.

**(4) General criteria for structural similarity**

a) The type chosen as representative for a group of types in relation to a given test may differ from period to period, depending on the types produced in that period.

b) For all relevant types in a group of types the same accelerated test procedure shall be allowed (see 4.9).

c) If, although fulfilling the particular criteria for a group, significant difference(s) still exist in characteristic(s), the type selected for the relevant test shall be represented by the most critical device, giving the greatest risk of failure for this test.

d) If failure occurs on a device type all the devices associated with this representative type are to be considered affected.

e) If the circuits are submitted to a screening procedure in accordance with 4.10, they may only be grouped if they are screened according to the same screening class. However, if several screening classes are applied in the same production line, the devices screened according to a given screening class are covered by devices unscreened or screened according to a lower screening class. For this purpose the screening classes as defined in 4.10 are given in the following order : D, E, F, C, B, H, where D is lowest one.

### 3.2.2 Test dependent criteria for structural similarity

The test dependent criteria for structural similarity applicable to the Group B and periodic tests are given in the following table.



Sub-clauses 3.2.2 (1) à 3.2.2 (18), specify the interpretation of these criteria.

**TEST DEPENDENT CRITERIA FOR STRUCTURAL SIMILARITY**

**(see note)**

| TESTS | Criteria | Assembly line 3.2.2 (1) | | Outline and dimensions of the package 3.2.2 (2) | Family of packages 3.2.2 (3) | Package material 3.2.2 (4) | Encapsulation methods 3.2.2 (5) | External terminals material 3.2.2 (6) | Finishing process 3.2.2 (7) | Marking 3.2.2 (8) | Number of terminals 3.2.2 (9) | | Material of internal connections, wire bonding 3.2.2 (10) | Die bonding 3.2.2 (11) | Ratio of die areas 3.2.2 (12) | | Diffusion line 3.2.2 (1) | Die manufacturing process 3.2.2 (13) | Density 3.2.2 (14) | Operating supply voltages 3.2.2 (15) | Operating temperature range 3.2.2 (16) | Functional and electrical criterion 3.2.2 (17) | Power dissipation 3.2.2 (18) b) | Power dissipation 3.2.2 (18) c) | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| B1 | Mains dimensions - Mass | X | | X | X | X | X | X | X | | | | | | | | | | | | | | | |
| B2 | Solderability | X | | | X | | X | X | X | | | | | | | | | | | | | | | |
| B3 | Sealing test (cavity packages) • | X | | | X | X | X | X | X | | X | | | | | | | | | | | | | |
| B4 | Change of temperature | X | | | X | X | X | X | | | X | | X | X | X | | | | | | | | | |
| B5 | Electrical endurance 168 h | X | | | X | X | X | X | X | | | | X | X | X | | X | X | X | X | X | X | X | |
| C1 | Secondary dimensions | X | | X | X | X | X | X | X | | | | | | | | | | | | | | | |
| C2 | Immersion in cleaning solvents | X | | | | X | X | | | X | | | | | | | | | | | | | | |
| C3 | Robustess of terminations | X | | | X | | X | X | X | | | | | | | | | | | | | | | |
| C4 | Resistance to soldering heat | X | | | X | X | X | X | | | X | | X | X | X | | | | | | | | | |
| C5 | Shock<br>Vibrations<br>Acceleration steady state | X | | | X | X | X | X | | | X | | X | X | X | | | | | | | | | |
| C6 | Damp heat (cavity packages) • | X | | | X | X | X | X | X | X | | | | | | | | | | | | | | |
| C7 | Damp heat (non cavity packages) | X | | | X | X | X | X | X | X | X | | X | X | X | | X | X | X | X | | | | X |
| C8 | Electrical endurance 2000 h | X | | | X | X | X | X | X | | | | X | X | X | | X | X | X | X | X | X | X | |
| C9 | Storage - Dry heat 1 000 h | X | | | X | X | X | X | X | X | | | X | X | | | X | X | | | | | | |
| C10 | Storage - Cold 1 000 h | X | | | X | X | X | X | X | X | | | X | X | | | X | X | | | | | | |
| C11a | Correlation - Dynamic tests at $T_{amb}$ max. | | | | | | | | | | | | | | | | X | X | X | X | X | X | X | |
| C11b | Correlation - Dynamic tests at $T_{amb}$ min. | | | | | | | | | | | | | | | | X | X | X | X | X | X | X | |
| C12a | Correlation - Functional tests at $T_{amb}$ max. | | | | | | | | | | | | | | | | X | X | X | X | X | X | X | |
| C12b | Correlation - Functional tests at $T_{amb}$ min. | | | | | | | | | | | | | | | | X | X | X | X | X | X | X | |

• cavity packages with non-organic sealing only