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INTERNATIONAL STANDARD

NORME INTERNATIONALE

Semiconductor devices – Hot carrier test on MOS transistors

Dispositifs à semiconducteurs – Essai de porteur chaud sur les transistors MOS

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The text of this standard is based on the following documents:

FDIS	Report on voting
47/2041/FDIS	47/2048/RVD

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

The committee has decided that the contents of this publication will remain unchanged until the stability date indicated on the IEC web site under "http://webstore.iec.ch" in the data related to the specific publication. At this date, the publication will be

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SEMICONDUCTOR DEVICES – HOT CARRIER TEST ON MOS TRANSISTORS

1 Scope

This standard describes the wafer level hot carrier test on NMOS and PMOS transistors. The test is intended to determine whether the single transistors in a certain (C)MOS process meet the required hot carrier lifetime.

2 Abbreviations and letter symbols

In this document the following abbreviations and letter symbols apply:

MOS	Metal Oxide Semiconductor
NMOS	n-channel MOS transistor
PMOS	p-channel MOS transistor
(C)MOS	Complementary MOS
L [µm]	length of polysilicon gate of MOS transistor
W [µm]	width of polysilicon gate of MOS transistor
$L_{nominal}$ [µm]	minimum L allowed by the design rules of the process
$W_{nominal}$ [µm]	minimum W allowed by the design rules of the process
V_{gs} [V]	gate-source voltage of MOS transistor
V_{ds} [V]	drain-source voltage of MOS transistor
V_{bs} [V]	backgate-source voltage of MOS transistor
I_{ds} [µA]:	drain-source current of MOS transistor
I_b [µA]	substrate current of MOS transistor
I_g [nA]	gate current of MOS transistor
$V_{gs,stress}$ [V]	V_{gs} biasing condition during hot carrier stress
$V_{ds,stress}$ [V]	V_{ds} biasing condition during hot carrier stress
V_{ds,use_max} [V]	maximum V_{ds} allowed by the design rules of the process as stated in the design manual
$V_{ds,breakdown}$ [V]	V_{ds} at which avalanche or punch-through currents become dominant; defined as V_{ds} at which I_{ds}= 1,5 × (I_{ds} at V_{ds,use_max}) while V_{gs}= V_{ds,use_max}
V_t [V]	threshold voltage of MOS transistor defined as V_{gs} voltage at which I_{ds}= 0,01 × W / L [µA]. Other (commonly agreed) definitions of V_t are also allowed as long as this is clearly reported.
g_m [µA/V]	transconductance of MOS transistor
$g_{m,max}$ [µA/V]	maximum transconductance of MOS transistor
$I_{ds,sat}$ [µA]	saturated drain-source current at V_{gs}= V_{ds}= $V_{ds,use\_,max}$; $I_{ds,sat\_forward}$ measured with source and drain having same polarity as during stress, $I_{ds,sat\_reverse}$ measured with source and drain polarity interchanged with respect to stress.
L(MOST)	length of the square MOS transistor (L = W)
$g_{m,max}$ (MOST)	$g_{m,max}$ of the square MOS transistor (L = W)

τ[s] lifetime of the MOS transistor

L_{eff} [µm] effective electrical channel length of MOS transistor; the L_{eff} for a given L is determined using the $g_{m,max}$ of a large 'square ( )' MOS transistor with $W = L >> L_{nominal}$.

3 Test structures

For the evaluation of the hot carrier degradation vulnerability of a technology, nominal transistors ($L = L_{nominal}$) are recommended. The following gate lengths are recommended when lifetime extrapolation versus L is needed (see 9.1): $L = 1{,}0 \times L_{nominal}$, $L = 1{,}5 \times L_{nominal}$, $L = 2{,}0 \times L_{nominal}$, $L = 5{,}0 \times L_{nominal}$, $L = W$.

Gates and sources of the transistors may be combined to reduce the number of bond pads required for these test structures.

Typical values for W are 10 µm for $L_{nominal} < 1$ µm, and 20 µm for $L_{nominal} \geq 1$µm. A transistor with small W (e.g. $W = L_{nominal}$) can be used to evaluate the occurrence of potential 'narrow width' effects.

The nominal transistor shall be placed with various orientations on the wafer (e.g. one with the orientation of its gate parallel to the flat of the wafer and one with its gate orientation perpendicular to the flat) whenever asymmetry effects due to ion implantation are expected.

4 Stress time

Typically 40 000 s (one night), in some 'low voltage' cases 200 000 s (1 weekend); readpoints logarithmically spaced (at least 3 per decade). Stress times shall be chosen such that the degradation exceeds at least 20 % of the maximum value for the selected failure criterion (see Clause 8).

5 Stress conditions

At least 3 different $V_{ds,stress}$ conditions where $V_{ds,stress\_max} < V_{ds,breakdown}$, $V_{bs} = 0$ V.

NMOS transistors are stressed at maximum substrate current conditions. Usually, the maximum substrate current occurs at approximately

$$V_{gs,stress} = V_{ds,stress} / 2\ \text{V} - 0{,}5\ \text{V} \quad (1)$$

If this is not the case for a certain technology, one shall determine the appropriate $V_{gs,stress}$ by substrate current measurements.

For deep-submicron transistors worst-case degradation may not occur at maximum substrate current, and it is therefore recommended that the worst-case stress conditions are checked.

PMOS transistors are stressed at maximum gate current conditions. Usually, maximum gate current occurs at approximately

$$V_{gs,stress} = V_t - 1{,}0\ \text{V} \quad (2)$$

(e.g. $V_t = -0{,}8$ V then $V_{gs} = -1{,}8$ V)

If this is not the case for a certain technology, one shall determine the appropriate $V_{gs,stress}$ by gate current measurements.

For accurate determination of the life time it is recommended to reach the failure criterion during the stress. This can be achieved by choosing a high V_{ds} value. A reasonable starting value is V_{ds}= 0,9 × $V_{ds,breakdown}$. If this is not feasible it is recommended to take at least two time decades of valid data and extrapolate to the failure criterion.

6 Sample size

The sample size is not prescribed. Too low sample sizes will result in short life times due to the 60 % confidence requirement for extrapolation.

It is recommended to use at least 3 V_{ds} bias conditions and 4 different W/L ratios.

The resulting number of datapoints is for example 3 (V_{ds}) × 4 (transistors) × 2 batches = 24 datapoints.

7 Temperature

Room temperature, kept constant within ±3 °C.

8 Failure criteria

Failure criteria have to be selected for one or more of the following parameters: $\Delta g_{m,max}$, ΔV_t, $\Delta I_{ds,sat\_forward}$, $\Delta I_{ds,sat\_reverse}$, $\Delta I_{ds,lin}$. Recommended criteria are given below:

$|\Delta g_{m,max}/g_{m,max}|$ = 10% at V_{ds}= 0,1 V or

$|\Delta V_t|$ = 0,02x$V_{dd,max}$ with a minimum value of 100 mV at V_{ds}= 0,1 V or

$|\Delta I_{ds,sat}/I_{ds,sat}|$forward = 10 % or

$|\Delta I_{ds,sat}/I_{ds,sat}|$reverse = 10 % or

$|\Delta I_{ds,lin}/I_{ds,lin}|$forward = 10 %

NMOS transistors typically show a decrease in g_m and $I_{ds,sat}$ and an increase in $|V_t|$.

PMOS transistors typically show an increase in g_m and $I_{ds,sat}$ and a decrease in $|V_t|$.

Lifetimes can be determined by interpolation and extrapolation of data. However it is recommended to disregard data where the shift in g_m, $I_{ds,sat}$ or V_t did not exceed 20 % of the failure criteria or when the data must be extrapolated by more than one decade in time in order to reach the failure criteria.

9 Lifetime estimation method

9.1 DC acceleration models

9.1.1 General

Two different methods for lifetime estimation are given. Method 1 uses the dependence of lifetime on the drain current, and requires only the nominal transistor. Method 2 uses the dependency of lifetime on gate length, and requires test structures with different *L*. Method 2 is used when the dependency of lifetime on channel length is needed.

9.1.2 Method 1: extrapolation vs. drain current

For NMOS transistors, extrapolation is done according to

$$\tau = A \times (I_b)^{-m} \quad (3)$$

where

A is a process-dependent constant, and

m is the substrate current acceleration exponent.

For $L < 0{,}5$ µm, a better fit may be obtained with [1][1]:

$$\tau^* I_{ds} = A \times (I_b/I_{ds})^{-m} \quad (4)$$

For PMOS transistors, extrapolation is done according to [2]:

$$\tau = A \times (I_g)^{-m} \quad (5)$$

The parameters A and m are found by plotting $\log(\tau)$ versus $\log(I_b)$ or $\log(I_g)$ (see equation 4 and equation 6 respectively), or by plotting $\log(\tau^* I_d)$ versus $\log(I_b/I_d)$ (see equation 5). A straight line is found with slope m and intercept $\log(A)$.

9.1.3 Method 2: extrapolation versus drain bias and channel length

For NMOS transistors, the Takeda model [3] can be used for the channel length dependence.

$$\tau = A \times \exp(B / V_{ds,stress}) \times (L_{eff})^C \quad (6)$$

where

A is a process-dependent constant;

B is the process-dependent voltage acceleration constant;

C is the process-dependent channel length acceleration constant.

L_{eff} is given by

$$L_{eff} = L(\ \text{MOST}) \times g_{m,max}(\ \text{MOST}) / g_{m,max}(L) \quad (7)$$

For PMOS transistors, the Woltjer model [4] can be used for the channel length dependence.

$$\tau = A \times \exp(B / V_{ds,stress}) \times \exp(C \times \sqrt{(L_{eff})}) \quad (8)$$

The parameters A, B and C are found from a simultaneous fit of the lifetime τ as a function of $V_{ds,stress}$ and L_{eff}.

For deep submicron CMOS technologies other extrapolation models are also used for the channel length dependence of lifetime for both NMOS en PMOS transistors, e.g. $\tau = A \times \exp(C x L_{eff})$ or $\tau = A \times \exp(C/L_{eff})$

NOTE In these models, only lifetime data based on one failure criterion should be used at a time.

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[1] The figures in square brackets refer to the Bibliography.

9.2 AC estimation model

For AC applications, lifetime is calculated according to

$$\tau_{AC} = \tau_{DC} \times t_{cycle}/(t_{rise}+t_{fall}) \quad (9)$$

where

τ_{AC} is the lifetime of the AC bias condition,

τ_{DC} the lifetime of the DC bias condition,

t_{cycle} is the cycle time of the AC stress,

t_{rise} is the rise time of the AC stress, and

t_{fall} is the fall time of the AC stress.

AC tests are recommended.

10 Lifetime requirements

In analog circuits, the required lifetime may be achieved by increasing the minimum L_{eff} allowed in analog designs.

Hot carrier lifetime of digital circuitry exceeds the static transistor lifetime by far due to duty cycle effects and limited sensitivity of digital circuitry to transistor degradation [5].

11 Reporting

The following items shall be reported as a minimum, when presenting hot carrier data:

– number of transistors used as well as their dimensions;

– stress voltages used;

– failure criterion which is reached first;

– values of the constants *A*, *B* and *C* as well as their sigma's;

– a plot of the lifetime as a function of $1/V_{ds}$ for all transistors used.