SLOVENSKI STANDARD
SIST EN 60191-6-6:2002

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Mechanical standardization of semiconductor devices - Part 6-6: General rules for the preparation of outline drawings of surface mounted semiconductor device package - Design guide for fine pitch land grid array (FLGA) (IEC 60191-6-6:2001)

Mechanical standardization of semiconductor devices -- Part 6-6: General rules for the preparation of outline drawings of surface mounted semiconductor device packages - Design guide for fine pitch land grid array (FLGA)

Mechanische Normung von Halbleiterbauelementen -- Teil 6-6: Allgemeine Regeln für die Erstellung von Gehäusezeichnungen von SMD-Halbleitergehäusen - Konstruktionsleitfaden für Feinraster-Land-Grid-Array (FLGA)

Normalisation mécanique des dispositifs à semi-conducteurs -- Partie 6-6: Règles générales pour la préparation des dessins d'encombrement des dispositifs à semiconducteurs pour montage en surface - Guide de conception des dispositifs FLGA

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01.100.25	Risbe s področja elektrotehnike in elektronike	Electrical and electronics engineering drawings
31.080.01	Polprevodniški elementi (naprave) na splošno	Semiconductor devices in general
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English version

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Teil 6-6: Allgemeine Regeln für die Erstellung von Gehäusezeichnungen von SMD-Halbleitergehäusen - Konstruktionsleitfaden für Feinraster-Land-Grid-Array (FLGA)
(IEC 60191-6-6:2001)

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CENELEC
European Committee for Electrotechnical Standardization
Comité Européen de Normalisation Electrotechnique
Europäisches Komitee für Elektrotechnische Normung

Central Secretariat: rue de Stassart 35, B - 1050 Brussels

Foreword

The text of document 47D/404/FDIS, future edition 1 of IEC 60191-6-6, prepared by SC 47D, Mechanical standardization of semiconductor devices, of IEC TC 47, Semiconductor devices, was submitted to the IEC-CENELEC parallel vote and was approved by CENELEC as EN 60191-6-6 on 2001-05-01.

The following dates were fixed:

- latest date by which the EN has to be implemented at national level by publication of an identical national standard or by endorsement (dop) 2002-02-01
- latest date by which the national standards conflicting with the EN have to be withdrawn (dow) 2004-05-01

Annexes designated "normative" are part of the body of the standard.
In this standard, annex ZA is normative.
Annex ZA has been added by CENELEC.

Endorsement notice

The text of the International Standard IEC 60191-6-6:2001 was approved by CENELEC as a European Standard without any modification.

INTRODUCTION

The demand for area array style packages exists because of the multi-functions and high performance of electrical equipment. The objective of this design guide is to standardize outlines and to get interchangeability of FLGA packages. The terminal pitch and package outlines of these fine-pitch array packages are smaller than those of LGA packages.

MECHANICAL STANDARDIZATION OF SEMICONDUCTOR DEVICES –

Part 6-6: General rules for the preparation of outline drawings of surface mounted semiconductor device packages – Design guide for fine-pitch land grid array (FLGA)

1 Scope

This part of IEC 60191 provides common outline drawings and dimensions for all types of structures and composed materials of fine-pitch land grid array (hereinafter called FLGA) whose terminal pitch is less than, or equal to, 0,80 mm and whose package body outline is square.

2 Normative references

The following normative documents contain provisions which, through reference in this text, constitute provisions of this part of IEC 60191. For dated references, subsequent amendments to, or revisions of, any of these publications do not apply. However, parties to agreements based on this part of IEC 60191 are encouraged to investigate the possibility of applying the most recent editions of the normative documents indicated below. For undated references, the latest edition of the normative document referred to applies. Members of IEC and ISO maintain registers of currently valid International Standards.

IEC 60191 (all parts), *Mechanical standardization of semiconductor devices*

3 Definitions

For the purposes of this part of IEC 60191, the following definitions, as well as those given in the other parts of this standard, apply.

3.1
flanged type
type whose package body size (body length and width) consists of its own flange composed around the encapsulation or lid

3.2
type of real chip size
type whose package body size (body length and width) consists of an encapsulation around the real chip only

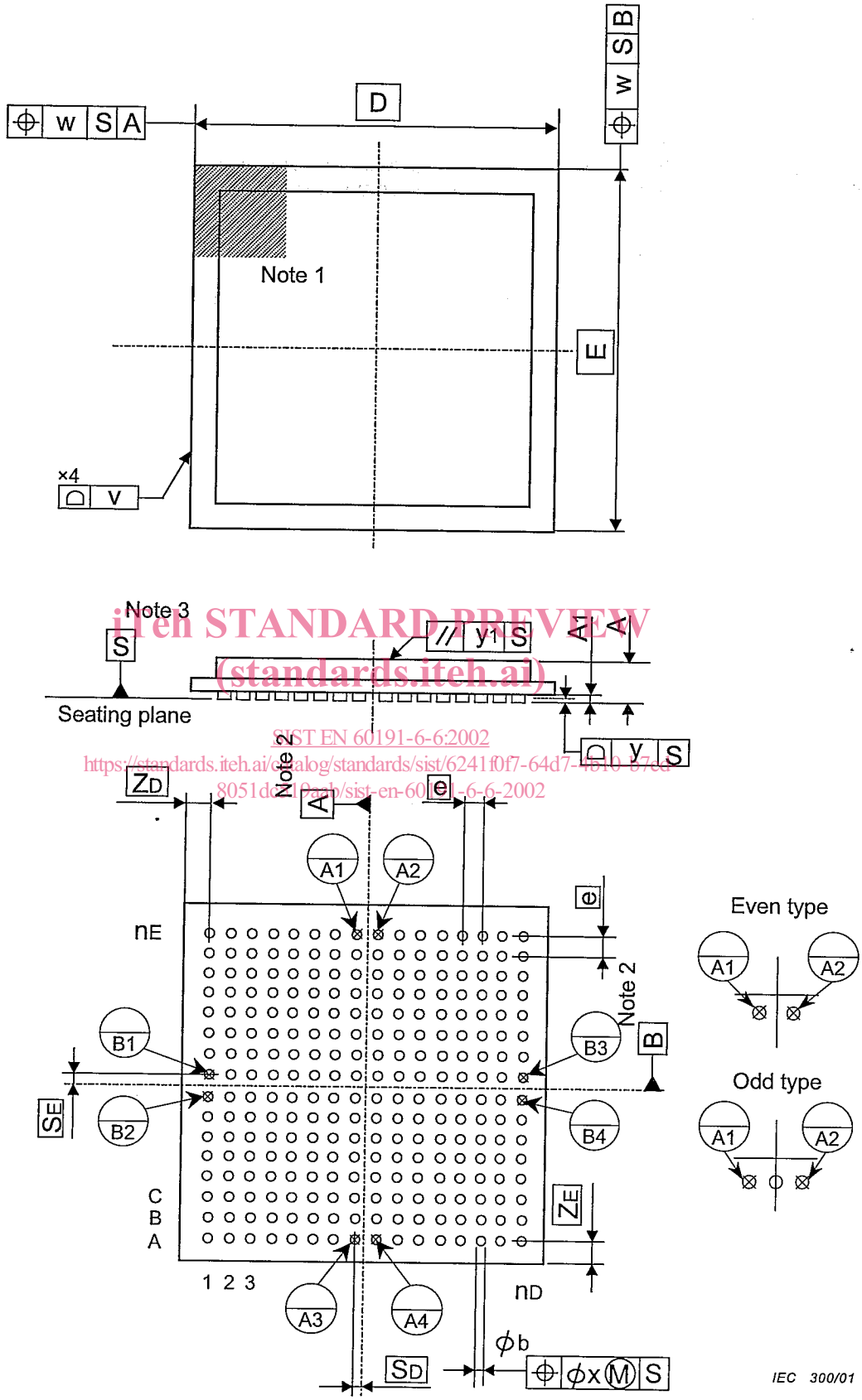
3.3
FLGA
packages with metal lands or metal bumps of which the terminal height is less than, or equal to, 100 µm, and whose terminal pitch is less than, or equal to, 0,80 mm, positioned in an array on the base plane of the package as external terminals

This package structure makes it possible to surface-mount the packages to the printed circuit board

3.4
material designation
FLGA packages are classified according to the following two material designations:

3.4.1
plastic type (P-FLGA)
plastic-type classification is assigned to packages which consist of resin substrate as interposer material (for example, glass-epoxy, poly-imid)

3.4.2
ceramic type (C-FLGA)
ceramic-type classification is assigned to packages which consist of ceramic substrate as interposer material



	Design guide for fine-pitch land grid array family **Fine-pitch land grid array family**	
	IEC 60191	

NOTE 1 Zone of a visible index on the top surface.

NOTE 2 Datum A and B are the axes defined by the terminal positions indicated with datum targets.

NOTE 3 Primary datum S and seating plane to be defined by the method of least squares of spherical crowns of terminals.