



Edition 2.1 2012-09 CONSOLIDATED VERSION

# INTERNATIONAL STANDARD

# NORME INTERNATIONALE



Semiconductor devices – Mechanical and climatic test methods – Part 27: Electrostatic discharge (ESD) sensitivity testing – Machine model (MM)

Dispositifs à semiconducteurs – Méthodes d'essais mécaniques et climatiques – Partie 27: Essai de sensibilité aux décharges électrostatiques (DES) – Modèle de machine (MM)

IEC 60/49-27:2006

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INTERNATIONAL ELECTROTECHNICAL COMMISSION

COMMISSION ELECTROTECHNIQUE INTERNATIONALE

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#### INTERNATIONAL ELECTROTECHNICAL COMMISSION

## SEMICONDUCTOR DEVICES – MECHANICAL AND CLIMATIC TEST METHODS –

## Part 27: Electrostatic discharge (ESD) sensitivity testing – Machine model (MM)

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IEC 60749-27 edition 2.1 contains the second edition (2006) [documents 47/1861/FDIS and 47/1873/RVD] and its amendment 1 (2012) [documents 47/2135/FDIS and 47/2144/RVD].

A vertical line in the margin shows where the base publication has been modified by amendment 1. Additions and deletions are displayed in red, with deletions being struck through.

International Standard IEC 60749-27 has been prepared by IEC technical committee 47: Semiconductor devices.

This second edition cancels and replaces the first edition, published in 2003, and has been revised in collaboration with technical committee 101. Whilst it does not contain any major technical changes, reference is now made, where necessary, to IEC 61340-3-2.

A list of all parts of IEC 60749 series, under the general title Semiconductor devices – Mechanical and climatic test methods can be found on the IEC website.

The committee has decided that the contents of the base publication and its amendments will remain unchanged until the stability date indicated on the IEC web site under "http://webstore.iec.ch" in the data related to the specific publication. At this date, the publication will be

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## SEMICONDUCTOR DEVICES – MECHANICAL AND CLIMATIC TEST METHODS –

## Part 27: Electrostatic discharge (ESD) sensitivity testing – Machine model (MM)

#### 1 Scope

This part of IEC 60749 establishes a standard procedure for testing and classifying semiconductor devices according to their susceptibility to damage or degradation by exposure to a defined machine model (MM) electrostatic discharge (ESD). It may be used as an alternative test method to the human body model ESD test method. The objective is to provide reliable, repeatable ESD test results so that accurate classifications can be performed.

This test method is applicable to all semiconductor devices and is classified as destructive.

ESD testing of semiconductor devices is selected from this test method, the human body model (HBM – see IEC 60749-26) or other test methods in the IEC 60749 series. The MM and HBM test methods produce similar but not identical results. Unless otherwise specified, the HBM test method is the one selected.

NOTE 1 This test method does not truly simulate discharge from real machines or metallic tools because the test method uses high parasitic inductance of the test circuit, whereas real machines and metallic tools, whose discharge rise time is approximately 100 ps, have no inductance.

NOTE 2 Certain clauses in this test method are in accordance with IEC 61340-3-2.

#### 2 Normative references

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 61340-3-2, Electrostatics – Part 3-2: Methods for simulation of electrostatic effects – Machine model (MM – Component testing ) electrostatic discharge test waveforms

IEC 60749-26: Semiconductor devices – Mechanical and climatic test methods – Part 26: Electrostatic discharge (ESD) sensitivity testing – Human body model (HBM)

#### 3 Terms and definitions

For the purposes of this document, the following terms and definitions apply.

#### 3.1

#### device under test

DUT

semiconductor product subjected to MM ESD test

#### 3.2

#### **DUT** failure

condition in which a DUT does not meet one or more specified parameters as a result of ESD test

#### 3.3

#### **ESD** withstand voltage

maximum applied ESD voltage level that does not cause failure parameter limits to be exceeded provided that all DUTs stressed at lower levels have also passed

NOTE Clause 3 of this test method is in accordance with IEC 61340-3-2 except for the specific reference to devices.

#### 3.4

#### ringing

noise component caused by a large inductance in the discharge circuit

#### 4 Equipment

#### 4.1 MM ESD waveform generator

This equipment produces an electrostatic discharge current pulse simulating a MM ESD event for application to the DUT. The equivalent waveform generator circuit and tester evaluation loads are illustrated in Figure 1.

#### 4.2 Waveform verification equipment

#### 4.2.1 General

Equipment capable of verifying the MM current waveform is defined in this standard. This equipment includes but is not limited to a waveform recording system, a high voltage resistor and a current transducer.

#### 4.2.2 Waveform recording system

The waveform recording system shall have a minimum single shot bandwidth of 350 MHz.

#### 4.2.3 Evaluation loads

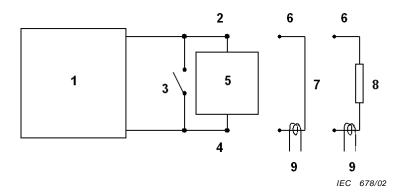
Two evaluation loads are necessary to verify the functionality of the waveform generator:

- a) load 1: a shorting wire;
- b) load 2: a 500  $\Omega$  with a tolerance of  $\pm 1$  % low inductance resistor appropriate rated for the voltages that will be used for waveform qualification.

The lead length of the evaluation loads (shorting wire or resistor) shall be as short as possible consistent with connecting the evaluation load to the appropriate reference terminals (A and B in Figure 1) while passing through the current transducer.

#### 4.2.4 Current transducer

The current transducer shall have a minimum bandwidth of 350 MHz.



#### Key

- 1 MM ESD waveform generator (nominally 200 pF)
- 2 Terminal A
- 3 Switch
- 4 Terminal B
- 5 DUT
- 6 Evaluation load
- 7 Shorting wire
- 8 Resistance  $R = 500 \Omega$
- 9 Current transducer

Figure 1 – MM ESD waveform generator equivalent

#### Requirements for Figure 1:

- 1. The evaluation loads (7 and 8) are specified in 4.2.3.
- 2. The current transducer (9) is specified in 4.2.4.
- 3. The reversal of terminals A (2) and B (4) to achieve dual polarity is not permitted.
- 4. The switch (3) is closed 10 ms to 100 ms after the pulse delivery period of each single MM pulse to ensure that the DUT and any test fixture are not left in a charged state.

NOTE 1 The performance of the waveform generator is strongly influenced by parasitic capacitance and inductance.

NOTE 2 Precautions must be taken in the design of the waveform generator to avoid recharge transients and double pulses.

NOTE 3 A resistance in series with the switch would ensure a slow discharge of the DUT.

NOTE 4 Clause 4 of this test method is in accordance with IEC 61340-3-2 except for the specific reference to devices.

#### 5 MM current waveform requirements

#### 5.1 General

Prior to DUT testing, MM ESD waveform generator qualification shall ensure waveform integrity of the discharge current through both a shorting wire and a resistive load. The shorting wire waveform requirements are specified in Figure 2 for all positive and negative voltages defined in Table 1, while the resistive load waveform requirements for  $\pm 400$  V are shown in Figure 3 and Table 1.

IEC 682/02

Table 1 – Waveform specification

Level	Equivalent voltage ∀	I <sub>p1</sub> peak current through a shorting wire A (±15 %)	$I_{\mbox{\footnotesize PR}}$ peak current through a 500 $\Omega$ resistor $\mathbb A$	$I_{100}$ current through a 500 $\Omega$ resistor at 100 ns A (±15 %)
1	<del>100</del>	1,7	-	-
2	<del>200</del>	<del>3,5</del>	-	-
3	<del>400</del>	<del>7,0</del>	< <i>I</i> <sub>100</sub> × 4,5	<del>0,29</del>
4	800	<del>14,0</del>	_	_

Level	Equivalent voltage	$I_{\rm p1}$ peak current through a shorting wire A $(\pm$ 15 %) $^{\rm a}$	$I_{PR}$ peak current through a 500 $\Omega$ resistor	$I_{100}$ current through a 500 $\Omega$ resistor at 100 ns A ( $\pm$ 15 $\%$ )		
1	100	1,7 (1,5)	_	_		
2	200	3,5 (3,0)	_	_		
3	400	7,0 (6,0)	< <i>I</i> <sub>100</sub> × 4,5	0,29		
4	800	14,0 (12,0)	-	-		
<sup>a</sup> Values in parentheses are the peak current value without ringing.						

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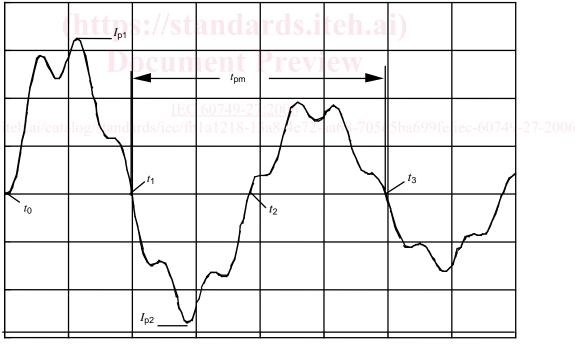


Figure 2 – Typical current waveform through a shorting wire

20 ns per division

https://standards.:

#### Requirements for Figure 2:

The current pulse shall meet the following requirements:

 $I_{\rm p1}$  is the maximum peak current is specified in Table 1;

 $I_{\rm p2}$  is the second peak current shall be between 67 % and 90 % of the absolute value obtained for  $I_{\rm p1}$  for each level;

 $t_{\rm pm}$  is the period of the major pulse shall be between 63 ns and 91 ns. The measurement shall be made between the first zero crossing point,  $t_{\rm 1}$ , and the third zero crossing point,  $t_{\rm 3}$ . The inductance (L) which is related to  $t_{\rm pm}$  shall be controlled to meet the above specified pulse period. The recommended value is 750 nH.



Figure 3 – Typical current waveform through a 500  $\Omega$  resistor

#### Requirements for Figure 3:

The current pulse through a 500  $\Omega$  resistor shall meet the following characteristics:

 $I_{PR}$  is the maximum peak current shall be within the range specified in Table 1;

 $I_{100}$  is the current at 100 ns is defined in Table 1.

#### 5.3 Extra consideration for waveform specifications

The peak current  $I_{\text{p1}}$  without ringing shall be verified against the values in Table 1.