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IEEE 1076.6™

VHDL Register Transfer Level (RTL) synthesis

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INTERNATIONAL ELECTROTECHNICAL COMMISSION

VHDL REGISTER TRANSFERT LEVEL (RTL) SYNTHESIS

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International Standard IEC/IEEE 62050 has been processed through IEC technical committee 93: Design automation.

The text of this standard is based on the following documents:

IEEE Std	FDIS	Report on voting
1076.6 (2004)	93/212/FDIS	93/217/RVD

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directives.

The committee has decided that the contents of this publication will remain unchanged until 2009.

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IEEE Standard for VHDL Register Transfer Level (RTL) Synthesis

Sponsor

Design Automation Standards Committee
of the
IEEE Computer Society

Approved 25 August 2004

American National Standard Institute

Approved 12 May 2004

IEEE-SA Standards Board

Abstract: This document specifies a standard for use of very high-speed integrated circuit hardware description language (VHDL) to model synthesizable register-transfer level digital logic. A standard syntax and semantics for VHDL register-transfer level synthesis is defined. The subset of the VHDL language, which is synthesizable, is described, and nonsynthesizable VHDL constructs are identified that should be ignored or flagged as errors.
Keywords: hardware description language, logic synthesis, register transfer level (RTL), very high-speed integrated circuit hardware description language (VHDL)

IEEE Introduction

This standard describes a standard syntax and semantics for VHDL RTL synthesis. It defines the subset of IEC/IEEE 61691-1-1:2004 (VHDL) that is suitable for RTL synthesis and defines the semantics of that subset for the synthesis domain. This standard is based on IEC/IEEE 61691-1-1:2004, IEEE Std 1164™-1993, and IEEE Std 1076.3™-1997.

The purpose of this standard is to define a syntax and semantics that can be used in common by all compliant RTL synthesis tools to achieve uniformity of results in a similar manner to which simulation tools use IEC/IEEE 61691-1-1:2004. This will allow users of synthesis tools to produce well-defined designs whose functional characteristics are independent of a particular synthesis implementation by making their designs compliant with this standard.

The standard is intended for use by logic designers and electronic engineers.

This document specifies IEEE Std 1076.6-2004, which is a revision of IEEE Std 1076.6-1999. The VHDL Synthesis Interoperability Working Group (SIWG) of the IEEE Computer Society started the development of IEEE Std 1076.6-2004 in January 1998. The work initially started as a Level 2 effort (Level 1 being IEEE Std 1076.6-1999). In fact the work on Level 2 continued right after Level 1 was completed by the working group. The working group realized that a Level 2 was required and that it would take some time to develop and continued working on it at regular face-to-face meetings and teleconferences. As the Level 2 draft continued to mature, the working group decided that rather than having two different levels of synthesis subsets, it was better to just have one standard, with IEEE Std 1076.6-2004 becoming Level 2.

The intent of this version was to include a maximum subset of VHDL that could be used to describe synthesizable RTL logic. This included considering new features introduced by IEC/IEEE 61691-1-1:2004, new semantics based on algorithmic styles rather than template-driven, and a set of synthesis attributes that could be used to annotate an RTL description. The following team leaders drove this effort:

Syntax: Lance Thompson

Semantics: Vinaya Singh

Attributes: Sanjiv Narayan

In addition, the following provided much-needed additional support:

Web and reflector admin: David Bishop

Documentation: John Michael Williams

A majority of the work conducted by the working group was done via teleconferencing, which was held regularly and open to all. Also, the working group used an e-mail reflector and its web page effectively to distribute and share information.

The following volunteers contributed to the development of this standard:

J. Bhasker, *Chair*

Jim Lewis, *Vice-Chair*

Rob Anderson	Rich Hatcher	Jonas Nilsson
Bill Anker	Mohammad Kakoee	Alain Raynaud
Victor Berman	Masamichi Kawarabayashi	Mehrdad Reshadi
David Bishop	Apurva Kalia	Fredj Rouatbi
Dominique Borrione	Satish Kumar	Steve Schultz
Dennis Brophy	Evan Lavelle	Manish Shrivastava
Andrew Brown	Vijay Madisetti	Vinaya Singh
Patrick Bryant	Erich Marschner	Douglas Smith
Ben Cohen	Paul Menchini	Lance Thompson
Tim Davis	Amitabh Menon	Alessandro Uber
Colin Dente	Egbert Molenkamp	Jim Vellenga
Wolfgang Ecker	Bob Myers	Eugenio Villar
Bob Flatt	Sanjana Nair	John Michael Williams
Christopher Grimm	Sanjiv Narayan	Francisco De Ycaza
Steve Grout	Zain Navabi	Alex Zamfirescu

Development of IEEE Std 1076.6-1999

Initial work on this standard started as a synthesis interoperability working group under VHDL International. The working group was also chartered by the EDA Industry Council Project Technical Advisory Board (PTAB) to develop a draft based on the donated subsets by the following companies/groups:

— Cadence

— European Synthesis Working Group

— IBM

— Mentor Graphics

— Synopsys

After the PTAB approved of the draft 1.5 with an overwhelming affirmative response, an IEEE PAR was obtained to clear its way for IEEE standardization. Most of the members of the original group continued to be part of the Pilot Group under P1076.6 to lead the technical work.

At the time the 1999 standard was completed, the P1076.6 Pilot Team had the following membership:

Rob Anderson	Wolfgang Ecker	Doug Perry
Victor Berman	Bob Flatt	Steve Schultz
J. Bhasker	Christopher Grimm	Doug Smith
David Bishop	Rich Hatcher	Lance Thompson
Dominique Borrione	Apurva Kalia	Fur-Shing Tsai
Dennis Brophy	Masamichi Kawarabayashi	Jim Vellenga
Ben Cohen	Jim Lewis	Eugenio Villar
Colin Dente	Sanjiv Narayan	Nels Vander Zanden

Many individuals from different organizations contributed to the development of this standard. In particular, in addition to the Pilot Team, the following individuals contributed to the development of the standard by being part of the working group:

Bill Anker	Robert Blackburn	John Hillawi
LaNae Avra		Pradip Jha

In addition, 95 individuals on the working group e-mail reflector also contributed to this development.

Notice to users

Errata

Errata, if any, for this and all other standards can be accessed at the following URL: http://standards.ieee.org/reading/ieee/updates/errata/index.html. Users are encouraged to check this URL for errata periodically.

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VHDL REGISTER TRANSFER LEVEL (RTL) SYNTHESIS

1. Overview

1.1 Scope

This standard defines a subset of very high-speed integrated circuit hardware description language (VHDL) that ensures portability of VHDL descriptions between register transfer level synthesis tools. Synthesis tools may be compliant and yet have features beyond those required by this standard. This standard defines how the semantics of VHDL shall be used, for example, to model level-sensitive and edge-sensitive logic. It also describes the syntax of the language with reference to what shall be supported and what shall not be supported for interoperability.

Use of this standard should minimize the potential for functional simulation mismatches between models before they are synthesized and after they are synthesized.

1.2 Compliance to this standard

1.2.1 Model compliance

A VHDL model shall be defined as being compliant to this standard if the model

a) Uses only constructs described as supported or ignored in this standard

b) Adheres to the semantics defined in this standard

1.2.2 Tool compliance

A synthesis tool shall be defined as being compliant to this standard if it

a) Accepts all models that adhere to the model compliance definition defined in 1.2.1

b) Supports language related pragmas defined by this standard

c) Produces a circuit model that has the same functionality as the input model based on the verification process as outlined in Clause 5.

1.3 Terminology

The word *shall* indicates mandatory requirements strictly to be followed in order to conform to the standard and from which no deviation is permitted (*shall* equals *is required to*). The word *should* is used to indicate that a certain course of action is preferred but not necessarily required; or that (in the negative form) a certain course of action is deprecated but not prohibited (*should* equals *is recommended that*). The word *may* indicates a course of action permissible within the limits of the standard (*may* equals *is permitted*).

A synthesis tool is said to *accept* a VHDL construct if it allows that construct to be legal input; it is said to *interpret* the construct (or to provide an *interpretation* of the construct) by producing something that represents the construct. A synthesis tool is not required to provide an interpretation for every construct that it accepts, but only for those for which an interpretation is specified by this standard.

The constructs in the standard shall be categorized as follows:

Supported: RTL synthesis shall interpret a construct, that is, map the construct to an equivalent hardware representation.

Ignored: RTL synthesis shall ignore the construct and produce a warning. Encountering the construct shall not cause synthesis to fail, but synthesis results may not match simulation results. The mechanism, if any, by which RTL synthesis notifies (warns) the user of such constructs is not defined by this standard. Ignored constructs may include unsupported constructs.

Not Supported: RTL synthesis does not support the construct. RTL synthesis does not expect to encounter the construct, and the failure mode shall be undefined. RTL synthesis may fail upon encountering such a construct. Failure is not mandatory; more specifically, RTL synthesis is allowed to treat such a construct as ignored.

NOTE—A synthesis tool may interpret constructs that are identified as not supported in this standard. However a model that contains such unsupported constructs is not compliant with this standard.[1]

1.4 Conventions

This standard uses the following conventions:

a) The body of the text of this standard uses **boldface** to denote VHDL reserved words (such as **downto**).

b) The text of the VHDL examples and code fragments is represented in a fixed-width font.

c) Syntax text that is struck-through (e.g., ~~text~~) refers to syntax that shall not be supported.

d) Syntax text that is underscored (e.g., text) refers to syntax that shall be ignored.

e) < and > pairs are used to represent text in one of several different, but specific forms. For example, one of the forms of <clock_edge> could be “CLOCK'EVENT and CLOCK = '1'”.

f) Any paragraph starting with “NOTE—” is informative and not part of the standard.

g) The examples that appear in this document under “*Example:*” are for the sole purpose of demonstrating the syntax and semantics of VHDL for synthesis. It is not the intent of this standard to demonstrate, recommend, or emphasize coding styles that are more (or less) efficient in generating an equivalent hardware representation. In addition, it is not the intent of this standard to present examples that represent a compliance test suite, or a performance benchmark, even though these examples are compliant to this standard (except as noted otherwise).

[1]Notes in text, tables, and figures are given for information only and do not contain requirements needed to implement the standard.

2. References

This standard shall be used in conjunction with the following publications. When the following standards are superseded by an approved revision, the revision shall apply.

IEEE Std 1076.3™-1997, IEEE Standard Synthesis Packages (NUMERIC_BIT and NUMERIC_STD).[2, 3]

IEEE Std 1164™-1993, IEEE Standard Multivalue Logic System for VHDL Model Interoperability (STD_LOGIC_1164).

IEC/IEEE 61691-1-1:2004, Behavioural languages - Part 1-1: VHDL language reference manual[4]

3. Definitions and acronyms

3.1 Definitions

For the purposes of this standard, the following terms and definitions apply. *The Authoritative Dictionary of IEEE Standards Terms, Seventh Edition* should be referenced for terms not defined in this clause. Terms used within this standard but not defined in this clause are assumed to be from IEC/IEEE 61691-1-1:2004, IEEE Std 1164-1993, or IEEE Std 1076.3-1997.[5]

3.1.1 assignment reference: The occurrence of a literal or expression as the waveform element of a signal assignment statement or as the right-hand side expression of a variable assignment statement.

3.1.2 combinational logic: Logic that settles to a state entirely determined by the current input values and therefore that cannot store information. Any change in the input causes a new state completely defined by the new inputs.

3.1.3 don't care value: The enumeration literal '-' of the type STD_ULOGIC (or subtype STD_LOGIC).

3.1.4 edge-sensitive storage element: Any storage element mapped to by a synthesis tool that

a) Propagates the value at the data input whenever an appropriate transition in value is detected on a clock control input

b) Preserves the last value propagated at all other times, except when any asynchronous control inputs become active (for example, a flip-flop)

3.1.5 high-impedance value: The enumeration literal 'Z' of the type STD_ULOGIC (or subtype STD_LOGIC).

3.1.6 level-sensitive storage element: Any storage element mapped to by a synthesis tool that

a) Propagates the value at the data input whenever an appropriate value is detected on a clock control input

b) Preserves the last value propagated at all other times, except when any asynchronous control inputs become active (for example, a latch)

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[4]IEC/IEEE publications are also available from the Institute of Electrical and Electronics Engineers.

[5]Information on references can be found in Clause 2.

3.1.7 logical operation: An operation for which the VHDL operator is **and**, **or**, **nand**, **nor**, **xor**, **xnor**, or **not**.

3.1.8 metacomment: A VHDL comment (--) that is used to provide synthesis-specific interpretation by a synthesis tool.

3.1.9 metalogical value: One of the enumeration literals 'U', 'X', 'W', or '-' of the type STD_ULOGIC (or subtype STD_LOGIC).

3.1.10 pragma: A generic term used to define a construct with no predefined language semantics that influences how a synthesis tool will synthesize VHDL code into an equivalent hardware representation.

3.1.11 sequential logic: Logic that settles to a state not determined solely by current inputs. The current state of such logic can be determined only by knowing the current inputs and some history of past inputs in their sequential order. Sequential logic always stores information from past input and therefore may be used to implement storage elements.

3.1.12 synchronous assignment: An assignment that takes place when a signal or variable value is updated as a direct result of a clock edge expression evaluating as true.

3.1.13 synthesis library: A library of digital design objects such as logic gates, chip pads, memory blocks, or other blocks; instances of these elements are connected together by a synthesis tool to create a synthesized netlist.

3.1.14 synthesis tool: Any system, process, or tool that interprets register transfer level VHDL source code as a description of an electronic circuit and derives a netlist description of that circuit.

3.1.15 synthesis-specific attribute: An attribute recognized by a tool compliant to this standard.

3.1.16 user: A person, system, process, or tool that generates the VHDL source code that a synthesis tool processes.

3.1.17 vector: A one-dimensional array.

3.1.18 well-defined: Containing no metalogical or high-impedance value.

3.2 Acronyms

LRM The IEEE VHDL language reference manual, that is, IEC/IEEE 61691-1-1:2004.

RTL The register transfer level of modeling circuits in VHDL for use with register transfer level synthesis. Register transfer level is a level of description of a digital design in which the clocked behavior of the design is expressly described in terms of data transfers between storage elements in sequential logic, which may be implied, and combinational logic, which may represent any computing or arithmetic-logic-unit logic. RTL modeling allows design hierarchy that represents a structural description of other RTL models.