SLOVENSKI STANDARD

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Delay and power calculation standards - Part 2: Pre-layout delay calculation specification for CMOS ASIC libraries (IEC 61523-2:2002)

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EUROPEAN STANDARD **EN 61523-2**

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English version

Delay and power calculation standards
Part 2: Pre-layout delay calculation specification for CMOS ASIC libraries
(IEC 61523-2:2002)

Calcul de puissance et de délai
Partie 2 : Spécification du calcul
du délai de pré-implantation
pour les librairies ASIC CMOS
(CEI 61523-2:2002)

Berechnung von Verzögerung und
Leistungsaufnahme beim Entwurf
von Chips
Teil 2: Vorgezogene Berechnung
der Verzögerung
für CMOS-ASIC-Bibliotheken
(IEC 61523-2:2002)

This European Standard was approved by CENELEC on 2002-07-01. CENELEC members are bound to comply with the CEN/CENELEC Internal Regulations which stipulate the conditions for giving this European Standard the status of a national standard without any alteration.

Up-to-date lists and bibliographical references concerning such national standards may be obtained on application to the Central Secretariat or to any CENELEC member.

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CENELEC members are the national electrotechnical committees of Austria, Belgium, Czech Republic, Denmark, Finland, France, Germany, Greece, Hungary, Iceland, Ireland, Italy, Luxembourg, Malta, Netherlands, Norway, Portugal, Slovakia, Spain, Sweden, Switzerland and United Kingdom.

CENELEC
European Committee for Electrotechnical Standardization
Comité Européen de Normalisation Electrotechnique
Europäisches Komitee für Elektrotechnische Normung

Central Secretariat: rue de Stassart 35, B - 1050 Brussels

Ref. No. EN 61523-2:2002 E

Foreword

The text of document 93/151/FDIS, future edition 1 of IEC 61523-2, prepared by IEC TC 93, Design automation, was submitted to the IEC-CENELEC parallel vote and was approved by CENELEC as EN 61523-2 on 2002-07-01.

The ASIC Library Representation Working Group of EIAL EDA Technical Committee also participated in the preparation of this standard.

This standard is a revision of the EIAJ [1)] document: ASIC Library Representation (ALR):1994.

The following dates were fixed:

– latest date by which the EN has to be implemented at national level by publication of an identical national standard or by endorsement	(dop)	2003-04-01
– latest date by which the national standards conflicting with the EN have to be withdrawn	(dow)	2005-07-01

Annexes designated "normative" are part of the body of the standard.
Annexes designated "informative" are given for information only.
In this standard, annex ZA is normative and annexes A to F are informative.
Annex ZA has been added by CENELEC.

Endorsement notice

The text of the International Standard IEC 61523-2:2002 was approved by CENELEC as a European Standard without any modification.

1) Electronic Industries Association of Japan.

Annex ZA
(normative)

Normative references to international publications with their corresponding European publications

This European Standard incorporates by dated or undated reference, provisions from other publications. These normative references are cited at the appropriate places in the text and the publications are listed hereafter. For dated references, subsequent amendments to or revisions of any of these publications apply to this European Standard only when incorporated in it by amendment or revision. For undated references the latest edition of the publication referred to applies (including amendments).

NOTE When an international publication has been modified by common modifications, indicated by (mod), the relevant EN/HD applies.

Publication	Year	Title	EN/HD	Year
IEEE 1481	1999	Integrated Circuit (IC) Delay and Power Calculation System	-	-

INTERNATIONAL STANDARD

IEC 61523-2

First edition
2002-05

Delay and power calculation standards –

Part 2:
pre-layout delay calculation specification for CMOS ASIC libraries

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CONTENTS

INTERNATIONAL ELECTROTECHNICAL COMMISSION

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DELAY AND POWER CALCULATION STANDARDS –

Part 2: Pre-layout delay calculation specification for CMOS ASIC libraries

FOREWORD

1) The IEC (International Electrotechnical Commission) is a worldwide organization for standardization comprising all national electrotechnical committees (IEC National Committees). The object of the IEC is to promote international co-operation on all questions concerning standardization in the electrical and electronic fields. To this end and in addition to other activities, the IEC publishes International Standards. Their preparation is entrusted to technical committees; any IEC National Committee interested in the subject dealt with may participate in this preparatory work. International, governmental and non-governmental organizations liaising with the IEC also participate in this preparation. The IEC collaborates closely with the International Organization for Standardization (ISO) in accordance with conditions determined by agreement between the two organizations.
2) The formal decisions or agreements of the IEC on technical matters express, as nearly as possible, an international consensus of opinion on the relevant subjects since each technical committee has representation from all interested National Committees.
3) The documents produced have the form of recommendations for international use and are published in the form of standards, technical specifications, technical reports or guides and they are accepted by the National Committees in that sense.
4) In order to promote international unification, IEC National Committees undertake to apply IEC International Standards transparently to the maximum extent possible in their national and regional standards. Any divergence between the IEC Standard and the corresponding national or regional standard shall be clearly indicated in the latter.
5) The IEC provides no marking procedure to indicate its approval and cannot be rendered responsible for any equipment declared to be in conformity with one of its standards.
6) Attention is drawn to the possibility that some of the elements of this International Standard may be the subject of patent rights. The IEC shall not be held responsible for identifying any or all such patent rights.

International Standard IEC 61523-2 has been prepared by IEC technical committee 93: Design automation.

The ASIC Library Representation Working Group of EIAL EDA Technical Committee also participated in the preparation of this standard.

This standard is a revision of the EIAJ[1] document: *ASIC Library Representation (ALR):1994.*

The text of this standard is based on the following documents:

FDIS	Report on voting
93/151/FDIS	93/153/RVD

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

This standard does not follow the rules for the structure of international standards given in Part 2 of the ISO/IEC Directives.

NOTE This standard has been reproduced without significant modification of its original content or drafting.

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[1] Electronic Industries Association of Japan.

IEC 61523 consists of the following parts, under the general title: *Delay and calculation standards:*

IEC 61523-1:2001, Part 1: *Integrated circuit delay and power calculation systems*

IEC 61523-2, Part 2: *Pre-layout delay calculation specification for CMOS ASIC libraries*

The committee has decided that the contents of this publication will remain unchanged until 2006. At this date, the publication will be

- reconfirmed;
- withdrawn;
- replaced by a revised edition, or
- amended.

DELAY AND CALCULATION STANDARDS –

Part 2: Pre-layout delay calculation specification for CMOS ASIC libraries

1. Scope and object

This standard specifies the pre-layout delay calculation method for CMOS1[1]ASIC[2] Libraries which contains cell based primitives and memories to be used during the pre-layout design phase of Logic simulation, Timing verification, and Logic synthesis.

The delay calculation method addressed in this standard consists of

1) Estimation of wire capacitance and

2) Delay calculation method based on tablelook-up.

With use of DCL and SDF, this delay calculation method helps the user have a unified timing model for various EDA tools in the pre-layout design phase.

This standard is consistent with existing standards and accepts existing standard formats, like SPEF, DCL, and SDF.

Scope of this standard covers the CMOS ASIC front end timing design for using logic synthesizer, simulators, timing verifiers.

The delay calculation method specified is based on the input slew rate calculation step and the port to port calculation step.

During these calculation steps, the table lookup method is used.

The table method of this standard specifies two interpolation methods for delay calculation. One is bi-linear interpolation which is widely used through the industry. Another is a linear interpolation using neighboring 3 points.

The nature of the delay value has monotonously increasing function of convex surface. This linear interpolation has a few percent of differences between linear interpolation and SPICE result.

2. Normative references

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies

IEEE Standard 1481:1999, *Integrated Circuit (IC) Delay and Power Calculation System.*

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[1] Complementary metal oxide semiconductor (CMOS).

[2] Application – Specific Integrated Circuits (ASIC).

3. **Relations with other companion standards activities**

The input to the delay calculator are net list and library.
The net list is described on either Verilog or VHDL.
The library consists of a functional part and a delay parameter part.
The functional part of the library is covered by Verilog or VHDL.

NOTE The delay parameter part of the library has not been standardized , because it depends strongly on the delay calculation method. EIAJ/ALR version1.1 described the delay calculation method , and the delay calculation method of EIAJ/ALR version1.1 is represented by DCL and DCL-PI standard(IEEE 1481).

This part of IEC 61523 specifies in detail a table look up calculation formula for CMOS ASIC library[1)].
The output of the delay calculator is a Standard Delay Format (SDF).

4. **Terms and Definitions**

capacitance of the net: Net means equipotential signal pins which will be connected by routing. The capacitance of the net is the capacitance of all the signal pins tha tare connected by routing.

CMOS: Complementary Metal Oxide Semiconductor.

DCL: Delay Calculation Language.
front end design: Logical design phase of ASIC design. Back end design means layout design.
gate: module containing only one output which is a simple boolean function of its inputs. Some basic simple boolean functions are and/or/not.
input slew rate: Slope of the input signal of the gate.In CMOS,the gate output delay is the function of its input slope of the signal.
load capacitance: Capacitance driven by gate. Usually it is separated into two items: i.e. wiring load capacitance and the sum of input load capacitance.
logic synthesizer: CAD package function performing the translation from RTL-level descriptions to Gate-level descriptions.
port to port delay: One meaning is pin to pin delay inside of gate. The other is pin to pin delay between gates.
pre-layout: Design phase before layout, i.e.logical design phase.
propagation delay: Traveling time of a given edge of a signal. Usually it is separated into two items: i.e.propagation delay inside a gate and propagation

1) This is not defined in EIAS/ARL version 1.1.

delay from the output of a gate to the input of another gate which is driven by it.

SDF: Standard Delay Format.

simulator: CAD package function of the circuit simulator based on behavior, network, and stimulus. There are Digital and Analog Simulators.

SPEF: Standard Parasitic Exchangeable Format.

SPICE: Simulation Program similar to the program with the same name developed at UC Berkeley. The simulation results are in terms of continuous waveforms representing current or voltage. It emphasizes Integrated Circuit timing and waveforms.

timing verifier: CAD package function that checks register to register timing violations of setup and hold time. Network description and clock timing are necessary.

transient timing group: Group of signal values. The delay will be definedwhen the signal changes from one value to the other.

5. **Pre-layout delay calculation method for CMOS ASIC libraries**

Timing design is the critical issue in sub-micron CMOS ASIC. This clause specifies the detail pre-layout delay calculation.

5.1 **Delay model**

When considering a sub-micron pre-layout (capacitance-based) timing model, two items should be considered, (1)port to port delay timing and (2) input slew rate effect.

In this model, it is necessary to first calculate the capacitance of wires, and then, calculate delays. As a first step of delay calculation, input slew rate is calculated, nd then, port to port delay can be calculated by using the input slew rate. Therefore, a two step approach is necessary as shown in Figure 1.