IEC 62258-5

Edition 1.0   2006-08

INTERNATIONAL STANDARD

NORME INTERNATIONALE

Semiconductor die products –
Part 5: Requirements for information concerning electrical simulation

Produits de puce de semiconducteurs –
Partie 5: Exigences pour les informations concernant la simulation électrique

IEC 62258-5:2006

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INTERNATIONAL ELECTROTECHNICAL COMMISSION

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FOREWORD

1) The International Electrotechnical Commission (IEC) is a worldwide organization for standardization comprising all national electrotechnical committees (IEC National Committees). The object of IEC is to promote international co-operation on all questions concerning standardization in the electrical and electronic fields. To this end and in addition to other activities, IEC publishes International Standards, Technical Specifications, Technical Reports, Publicly Available Specifications (PAS) and Guides (hereafter referred to as "IEC Publication(s)"). Their preparation is entrusted to technical committees; any IEC National Committee interested in the subject dealt with may participate in this preparatory work. International, governmental and non-governmental organizations liaising with the IEC also participate in this preparation. IEC collaborates closely with the International Organization for Standardization (ISO) in accordance with conditions determined by agreement between the two organizations.

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International Standard IEC 62258-5 has been prepared by IEC technical committee 47: Semiconductor devices.

This standard should be read in conjunction with IEC 62258-1 and IEC 62258-2.

This bilingual version (2012-07) corresponds to the monolingual English version, published in 2006-08.

The text of this standard is based on the following documents:

FDIS	Report on voting
47/1869/FDIS	47/1882/RVD

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

The French version of this standard has not been voted upon.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

The structure of IEC 62258, as currently conceived, consists of the following parts under the general title *Semiconductor die products*:

Part 1: Requirements for procurement and use

Part 2: Exchange data formats

Part 3: Recommendations for good practice in handling, packing and storage (Technical Report)

Part 4: Questionnaire for die users and suppliers (Technical Report) (in preparation)

Part 5: Requirements for information concerning electrical simulation

Part 6: Requirements for information concerning thermal simulation

Part 7: XML schema for data exchange (Technical Report) (in preparation)

Further parts may be added as required.

The committee has decided that the contents of this publication will remain unchanged until the maintenance result date indicated on the IEC web site under "http://webstore.iec.ch" in the data related to the specific publication. At this date, the publication will be

• reconfirmed;
• withdrawn;
• replaced by a revised edition, or
• amended.

iTeh STANDARD PREVIEW
(standards.iteh.ai)

INTRODUCTION

This standard is based on the work carried out in the ESPRIT 4th Framework project GOODDIE which resulted in the publication of the ES 59008 series of European specifications. Organisations that helped prepare this part of IEC 62258 includes the ESPRIT ENCAST project, the Die Products Consortium, JEITA, JEDEC and ZVEI.

SEMICONDUCTOR DIE PRODUCTS –

Part 5: Requirements for information concerning electrical simulation

1 Scope

This part of IEC 62258 has been developed to facilitate the production, supply and use of semiconductor die products, including:

– wafers;

– singulated bare die;

– die and wafers with attached connection structures;

– minimally or partially encapsulated die and wafers.

This part of IEC 62258 specifies the information required to facilitate the use of electrical data and models for simulation of the electrical behaviour and verification of the correct functionality of electronic systems that include bare semiconductor die, with or without connection structures, and/or minimally packaged semiconductor die. It is intended to assist all those involved in the supply chain for die devices to comply with the requirements of IEC 62258-1 and IEC 62258-2.

2 Normative references

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 62258-1, *Semiconductor die products – Part 1: Requirements for procurement and use*

IEC 62258-2, *Semiconductor die products – Part 2: Exchange data formats*

3 Terms and definitions

For the purposes of this document, the terms, definitions and acronyms as given in IEC 62258-1 apply.

4 General

To comply with IEC 62258-1, suppliers of die devices shall furnish information, which is necessary and sufficient for users of the devices at all stages of design, procurement, manufacture and test of products containing them.

Whilst it is expected that much of the information supplied will be in the public domain and available from such sources as manufacturers' data sheets, this standard does not place an obligation on a supplier to make information public. Any information that a supplier considers to be proprietary or commercially sensitive may be supplied under the terms of a non-disclosure agreement.

Requirements and recommendations provided in this standard apply to electrical simulation models used to perform the following simulations:

– analysis of the signal propagation within the electronic system;
– verification of the correct functionality of the electronic system;
– verification of the timing requirements;
– verification of the testability.

Supporting information on the use of electrical simulation models is provided in Annex A.

5 Requirements for information on electrical simulation models

5.1 Information on the electrical simulation model

5.1.1 General

Where a simulation model is provided, the information as defined in the following subclauses shall be given.

5.1.2 Model file name

The name of the file containing the model shall be given.

5.1.3 Creation date

The date on which the model file was created shall be given.

5.1.4 Model description

A description of the model shall be provided in sufficient detail for a user to understand its scope and apply the corresponding simulator correctly.

5.1.5 Model source

The source and originator of the model shall be stated.

5.1.6 Simulation program

The name(s) of the simulation program(s) that will accept the model file as valid input shall be given.

5.1.7 Program version

The version(s) of the simulation program(s) that are compatible with the given file shall be given.

5.1.8 Compliance level

The level(s) of the simulation program(s) with which the model file complies shall be given (for example SPICE level 3).

5.1.9 Model scope

The scope of the model shall be given, including any limitations in its use (for example VHDL behavioural model).

5.2 Information on device connectivity

5.2.1 General

The appropriate information, as data and/or model(s), describing the component's connectivity features or characteristics should be stated.

NOTE Examples of simulation models include IBIS (ANSI/EIA-656), SPICE, IMIC (JEITA ED-5302) and Touchstone.

The following parameters are important for bare die and low frequency devices where terminal-to-terminal interference can be disregarded.

5.2.2 Pad capacitance

The capacitance of the input, output, power and ground pads of the device should be stated. The node to which the capacitance is measured should also be stated.

5.2.3 Input buffer

The electrical model(s) of the input buffer(s) should be stated. The type and compliance level of the model(s) should also be stated.

5.2.4 Output buffer

The electrical model(s) of the output buffer(s) should be stated. The type and compliance level of the model(s) should also be stated, as required in 5.1.

5.2.5 ESD protection

A description of the ESD protection circuitry, if any, should be given. If an ESD model is provided, the type and compliance level of the model shall also be stated, as required in 5.1.

5.3 Information on the timing simulation model

The appropriate model(s) describing the component's behaviour in the time dimension should be provided. Where required by the simulator the model of the device should be provided as an electronic file, so that it can be directly used as input to the simulation program. This is primarily intended for digital devices.

NOTE Examples of timing simulation models include VITAL, VERILOG, IEEE 1029.1 Waveform and Vector Exchange Specification and IEC 61691-3-4, Timing expression in VHDL (in preparation).

5.4 Information on connection redistribution

5.4.1 General

Where the electrical connection points or terminals of the device have been modified or altered by use of one or more redistribution layers, information concerning the electrical parameters of any redistribution traces should be given. Information on multi-pin connections should be given in matrix form.

5.4.2 Redistribution trace resistance

The resistance of the redistribution traces, if any, with respect to the initial or original contact should be stated. Any assumed or known tolerances should also be stated.

5.4.3 Redistribution trace capacitance

The self and mutual capacitance of the redistribution traces, if any, should be stated, preferably in matrix form. Any assumed or known tolerances should also be stated.

5.4.4 Redistribution trace inductance

The self and mutual inductance of the redistribution traces, if any, should be stated, preferably in matrix form. Any assumed or known tolerances should also be stated.

5.5 Information on package terminals

5.5.1 General

Where the electrical connection points or terminals of the device have been modified by use of an alternate connection method, such as the addition of bumps, balls or bond-wires, information concerning the electrical parameters of any package terminals should be given. Information on multi-pin connections is to be given in matrix form. One suggested format for the matrix could be in CLGR (capacitance-inductance-conductance-resistance) format.

5.5.2 Terminal resistance

The resistance of the package terminal (wire, bump, lead or ball) with respect to the original terminal should be stated. Any assumed or known tolerances should also be stated.

5.5.3 Terminal capacitance

The self and mutual capacitance of the package terminal (wire, bump, lead or ball) should be stated, preferably in matrix form. Any assumed or known tolerances should also be stated.

5.5.4 Terminal inductance

The self and mutual inductance of the package terminal (wire, bump, lead or ball) should be stated, preferably in matrix form. Any assumed or known tolerances should also be stated.