JTC 1

INTERNATIONAL STANDARD

ISO/IEC 7816-3

First edition
1989-09-15

Identification cards — Integrated circuit(s) cards with contacts —

Part 3 :
Electronic signals and transmission protocols

Cartes d'identification — Cartes à circuit(s) intégré(s) à contacts —

Partie 3 : Signaux électroniques et protocoles de transmission

Reference number
ISO/IEC 7816-3 : 1989 (E)

Contents

Foreword

ISO (the International Organization for Standardization) and IEC (the International Electrotechnical Commission) together form a system for worldwide standardization as a whole. National bodies that are members of ISO or IEC participate in the development of International Standards through technical committees established by the respective organization to deal with particular fields of technical activity. ISO and IEC technical committees collaborate in fields of mutual interest. Other international organizations, governmental and non-governmental, in liaison with ISO and IEC, also take part in the work.

In the field of information technology, ISO and IEC have established a joint technical committee, ISO/IEC JTC1. Draft International Standards adopted by the joint technical committee are circulated to national bodies for approval before their acceptance as International Standards. They are approved in accordance with procedures requiring at least 75 % approval by the national bodies voting.

International Standard ISO/IEC 7816-3 was prepared by Joint Technical Committee ISO/IEC JTC1, *Information Technology*.

Introduction

This part of ISO/IEC 7816 is one of a series of standards describing the parameters for integrated circuit(s) cards with contacts and the use of such cards for international interchange.

These cards are identification cards intended for information exchange negociated between the outside and the integrated circuit in the card. As a result of an information exchange, the card delivers information (computation results, stored data), and/or modifies its content (data storage, event memorization).

During the preparation of this International Standard, information was gathered concerning relevant patents upon which application of this standard might depend. Relevant patents were identified in France and USA, the patent holder being Bull S.A. in each case. However, ISO cannot give authoritative or comprehensive information about evidence, validity or scope of patents or like rights.

The patent holder has stated that licences will be granted on appropriate terms to enable application of this part of ISO/IEC 7816, provided that those who seek licences agree to reciprocate.

Further information is available from:

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Identification cards – Integrated circuit(s) cards with contacts –

Part 3 :
Electronic signals and transmission protocols

1 Scope

This part of ISO/IEC 7816 specifies the power and signal structures, and information exchange between an integrated circuit(s) card and an interface device such as a terminal.

It also covers signal rates, voltage levels, current values, parity conventions, operation procedures, transmission mechanisms and communication with the integrated circuit(s) card.

It does not cover information and instruction content, such as identification of issuers and users, services and limits, security features, journaling and instruction definitions.

2 Normative references

The following standards contain provisions which, through reference in this text, constitute provisions of this part of ISO/IEC 7816.

At the time of publication, the editions indicated were valid. All standards are subject to revision, and parties to agreements based on this part of ISO/IEC 7816 are encouraged to investigate the possibility of applying the most recent editions of the standards listed below. Members of IEC and ISO maintain registers of currently valid International Standards.

ISO 1177 : 1985, *Information processing — Character structure for start/stop and synchronous character oriented transmission.*

ISO 7810 : 1985, *Identification cards — Physical characteristics.*

ISO 7816-1 : 1987, *Identification cards — Integrated circuit(s) cards with contacts — Part 1 : Physical characteristics.*

ISO 7816-2 : 1988, *Identification cards — Integrated circuit(s) cards with contacts — Part 2 : Dimensions and location of the contacts.*

3 Definitions

The term identification card is defined in ISO 7810. For the purpose of this part of ISO/IEC 7816, the following definitions apply :

Interface device : A terminal, communication device or machine to which the integrated circuit(s) card is electrically connected during operation.

State H : High state logic level.

State L : Low state logic level.

State Z : Mark (as defined in ISO 1177).

State A : Space (as defined in ISO 1177).

'XY' : Hexadecimal notation, equal to XY to the base 16.

4 Electrical characteristics of the contacts

4.1 Electrical functions

Contacts assignments are specified in ISO 7816-2, supporting at least the following electrical circuits :

I/O : Input or output for serial data to the integrated circuit inside the card.

VPP : Programming voltage input (optional use by the card).

GND : Ground (reference voltage).

CLK : Clocking or timing signal (optional use by the card).

RST : Either used by itself (reset signal supplied from the interface device) or in combination with an additional internal reset control circuit (optional use by the card). If internal reset is implemented, the voltage supply on VCC is mandatory.

VCC : Power supply input (optional use by the card).

NOTE — The use of two remaining contacts will be defined in the appropriate application standards.

4.2 Voltage and current values

4.2.1 Measurement conventions

All measurements are defined with respect to contact GND and in an ambient temperature range of 0° C to 50° C.

All currents flowing into the card are considered positive.

All timings shall be measured relative to the appropriate threshold levels as defined in 4.2.3 to 4.2.7.

A contact is inactive when it remains between 0 V and 0,4 V referenced to contact GND for currents less than 1 mA.

4.2.2 Abbreviations

V_{IH}	High level input voltage	I_{IH}	High level input current
V_{IL}	Low level input voltage	I_{IL}	Low level input current
V_{CC}	Power supply voltage at VCC	I_{CC}	Supply current at VCC
V_{PP}	Programming voltage at VPP	I_{PP}	Programming current at VPP
V_{OH}	High level output voltage	I_{OH}	High level output current
V_{OL}	Low level output voltage	I_{OL}	Low level output current
t_R	Rise time between 10 % and 90 % of signal amplitude	C_{IN}	Input capacitance
t_F	Fall time between 90 % and 10 % of signal amplitude	C_{OUT}	Output capacitance

4.2.3 I/O

This contact is used as input (reception mode) or output (transmission mode) for data exchange. Two possible states exist for I/O :

— mark or high state (state Z), if the card and the interface device are in reception mode or if this state is imposed by the transmitter ;

— space or low state (state A), if this state is imposed by the transmitter.

When the two ends of the line are in reception mode, the line shall be maintained in state Z. When the two ends are in non-matched transmit mode, the logic state of the line may be indeterminate. During operation, the interface device and the card shall not both be in transmit mode.

Table 1 — Electrical characteristics of I/O under normal operation conditions

Symbol	Conditions		Minimum	Maximum	Unit
V_{IH}	Either	$I_{IH\,max} = \pm 500\ \mu A$	2	V_{CC}	V
	or [1]	$I_{IH\,max} = \pm 20\ \mu A$	0,7 x V_{CC}	V_{CC} [3]	V
V_{IL}	$I_{IL\,max} = -1$ mA		0 [3]	0,8	V
V_{OH} [2]	Either	$I_{OH\,max} = -100\ \mu A$	2,4	V_{CC}	V
	or	$I_{OH\,max} = -20\ \mu A$	3,8	V_{CC}	V
V_{OL}	$I_{OL\,max} = 1$ mA		0	0,4	V
t_R t_F	$C_{IN} = 30$ pF ; $C_{OUT} = 30$ pF			1	µs

1) For the interface device, take into account both conditions.
2) It is assumed that a pull-up resistor is used in the interface device (recommended value : 20 kΩ).
3) The voltage on I/O shall remain between -0,3 V and V_{CC}+0,3 V.

4.2.4 VPP

This contact may be used to supply the voltage required to program or to erase the internal non-volatile memory. Two possible states exist for VPP : idle state and active state, as defined in table 2. The idle state shall be maintained by the interface device unless the active state is required.

Table 2 — Electrical characteristics of VPP under normal operation conditions

Symbol	Conditions	Minimum	Maximum	Unit
V_{PP} I_{PP}	**Idle State** (programming non active)	0,95 x V_{CC}	1,05 x V_{CC} 20	V mA
V_{PP} I_{PP}	**Active State** (programming the card)	0,975 x P	1,025 x P I	V mA
The card provides the interface device with the values of P and I (default values : P = 5 and I = 50). See 6.1.4.4.				

Rise or fall time : 200 µs maximum. The rate of change of V_{PP} shall not exceed 2 V/µs.

The maximum power V_{PP} x I_{PP} shall not exceed 1,5 W when averaged over any period of 1 s.

4.2.5 CLK

The actual frequency, delivered by the interface device on CLK, is designated either by f_i the initial frequency during the answer to reset, or by f_s the subsequent frequency during subsequent transmission. For frequency values, see 6.1.4.4.

Duty cycle for asynchronous operation shall be between 45 % and 55 % of the period during stable operation. Care shall be taken when switching frequencies (from f_i to f_s) to ensure that no pulse is shorter than 45 % of the shorter period.

Table 3 — Electrical characteristics of CLK under normal operation conditions

Symbol	Conditions		Minimum	Maximum	Unit
V_{IH}	Either	$I_{IH\,max}$ = ± 200 µA	2,4	V_{CC} 2)	V
	or 1)	$I_{IH\,max}$ = ± 20 µA	0,7 x V_{CC}	V_{CC} 2)	V
	or 1)	$I_{IH\,max}$ = ± 10 µA	V_{CC} - 0,7	V_{CC} 2)	V
V_{IL}	$I_{IL\,max}$ = ± 200 µA		0 2)	0,5	V
t_R t_F	C_{IN} = 30 pF			9 % of period with a maximum of 0,5 µs	
1) For the interface device, take into account the three conditions. 2) The voltage on CLK shall remain between -0,3 V and V_{CC}+0,3 V.					

4.2.6 RST

The reset signal at RST is delivered according to subclause 5.2.

Table 4 — Electrical characteristics of RST under normal operation conditions

Symbol	Conditions		Minimum	Maximum	Unit
V_{IH}	Either or [1]	$I_{IH\,max}$ = ± 200 µA	4	V_{CC} [2]	V
		$I_{IH\,max}$ = ± 10 µA	V_{CC} - 0,7	V_{CC} [2]	V
V_{IL}		$I_{IL\,max}$ = ± 200 µA	0 [2]	0,6	V

1) For the interface device, take into account both conditions.
2) The voltage on RST shall remain between -0,3 V and V_{CC}+0,3 V.

4.2.7 VCC

This contact is used to supply the power voltage V_{CC}.

Table 5 — Electrical characteristics of VCC under normal operation conditions

Symbol	Minimum	Maximum	Unit
V_{CC}	4,75	5,25	V
I_{CC}		200	mA

5 Operating procedure for integrated circuit(s) cards

This operating procedure applies to every integrated circuit(s) card with contacts.

The dialogue between the interface device and the card shall be conducted through the consecutive operations :

— connection and activation of the contacts by the interface device ;

— reset of the card ;

— answer to reset by the card ;

— subsequent information exchange between the card and the interface device ;

— deactivation of the contacts by the interface device.

These operations are specified in the following subclauses.

NOTE — An active state on VPP should only be provided and maintained when requested by the card.

5.1 Connection and activation of the contacts

The electrical circuits shall not be activated until the contacts are connected to the interface device so as to avoid possible damage to any card meeting these standards.

The activation of the contacts by the interface device shall consist of the consecutive operations :

— RST is in state L ;

— VCC shall be powered ;

— I/O in the interface device shall be put in reception mode ;

— VPP shall be raised to idle state ;

— CLK shall be provided with a suitable and stable clock. See 4.2.5.

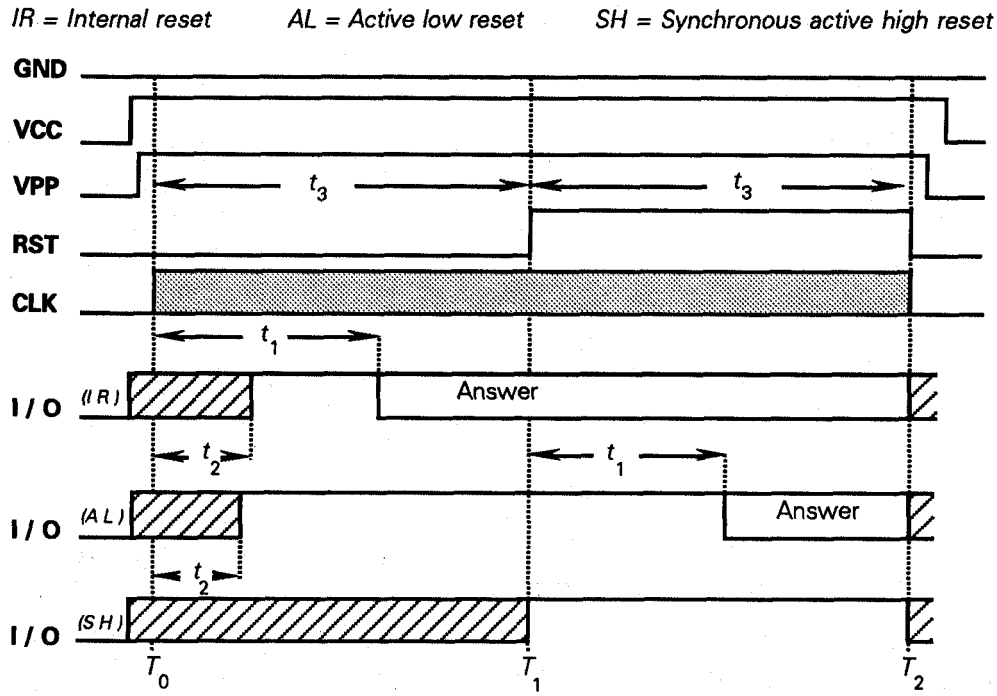


Figure 1 — Reset of the card

NOTE — The hatched area indicates a period when the state of I/O is undefined.

5.2 Reset of the card

A card reset is initiated by the interface device, whereupon the card shall respond with an Answer-to-Reset as described in clause 6.

By the end of the activation of the contacts (RST in state L, VCC powered and stable, I/O in reception mode in the interface device, VPP stable at idle state, CLK provided with a suitable and stable clock), the card **answering asynchronously** is ready for reset. See figure 1.

The clock signal is applied to CLK at time T_0. The I/O line shall be set to state Z within 200 clock cycles of the clock signal (t_2) being applied to CLK (time t_2 after T_0).

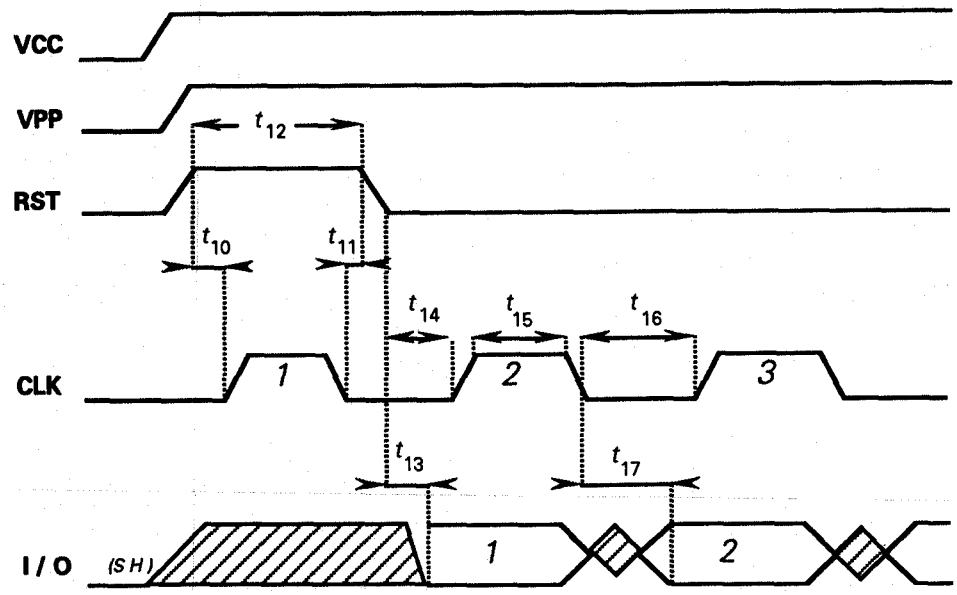
An internally reset card is reset after a few cycles of the clock signal. The Answer-to-Reset on I/O shall begin between 400 and 40 000 clock cycles (t_1) after the clock signal is applied to CLK (time t_1 after T_0).

A card with an active low reset is reset by maintaining RST in state L for at least 40 000 clock cycles (t_3) after the clock signal is applied to CLK (time t_3 after T_0). Thus, if no Answer-to-Reset begins within 40 000 clock cycles (t_3) with RST in state L, RST is put to state H (at time T_1). The Answer-to-Reset on I/O shall begin between 400 and 40 000 clock cycles (t_1) after the rising edge of the signal on RST (time t_1 after T_1).

If the Answer-to-Reset does not begin within 40 000 clock cycles (t_3) with RST in state H (t_3 after T_1), the signal on RST shall be returned to state L (at time T_2) and the contacts shall be deactivated by the interface device. See subclause 5.4.

With **a card answering synchronously**, the interface device sets all lines to state L. See figure 2. VCC is then powered, VPP is set to idle state, CLK and RST remain in state L, I/O is put in reception mode in the interface device. RST shall be maintained in state H for at least 50 µs (t_{12}), before returning to state L again.

The clock pulse is applied after an interval (t_{10}) from the rising edge of the reset signal. The duration for the state H of the clock pulse can be any value between 10 µs and 50 µs ; no more than one clock pulse during reset high is allowed. The time interval between the falling edges on CLK and RST is t_{11}.



5 µs ≤ t_{10}
5 µs ≤ t_{11}
50 µs ≤ t_{12} ..... Reset high
t_{13} ≤ 10 µs ..... Propagation delay
10 µs ≤ t_{14} ≤ 100 µs ..... Clock low after reset
10 µs ≤ t_{15} ≤ 50 µs ..... Clock high
10 µs ≤ t_{16} ≤ 100 µs ..... Clock low
t_{17} ≤ 10 µs ..... Propagation delay

Figure 2 — Reset of a card when a synchronous answer is expected

The first data bit is obtained as an answer on I/O while CLK is in state L and is valid after an interval t_{13} from the falling edge on RST.

NOTES

1 The internal state of the card is assumed not to be defined before reset. Therefore the design of the card has to avoid improper operation.

2 In order to continue the dialogue with the card, RST shall be maintained in the state where an answer occurs on I/O.

3 Reset of a card can be initiated by the interface device at its discretion at any time.

4 Interface devices may support one or more of these types of reset behaviour. The priority of testing for asynchronous or synchronous cards is not defined in this standard.

5.3 Answer-to-Reset and subsequent information exchange

The card answers after reset with a sequence defined in clause 6.

All data exchanged over the I/O circuit correspond to the execution of commands (via RST for reset and via I/O for any other command).

As for Answer-to-Reset, the operating procedure of commands (except those commands to be specified in the next part of ISO/IEC 7816) depends on the type of transmission (asynchronous or synchronous) and on the protocol type.

NOTES

1 The asynchronous half duplex character transmission protocol, with the interface device as the master, is specified in clause 8, the asynchronous half duplex block transmission protocol in clause 9. Further protocol types between the card and the interface device are for further study.

2 The interindustry commands for interchange are to be specified in the next part of ISO/IEC 7816. Application specific commands are specified either in existing standards or in additional standards to be defined.

5.4 Deactivation of the contacts

When information exchange is terminated or aborted (unresponsive card or detection of card removal), the electrical contacts shall be deactivated.

The deactivation by the interface device shall consist of the consecutive operations :

— State L on RST ;
— State L on CLK ;
— VPP inactive ;
— State A on I/O ;
— VCC inactive.

6 Answer-to-Reset

Two types of transmission are considered :

Asynchronous transmission

In this type of transmission, characters are transmitted on the I/O line in an asynchronous half duplex mode. Each character includes an 8-bit byte. See 6.1.2.

Synchronous transmission

In this type of transmission, a series of bits is transmitted on the I/O line in half duplex mode in synchronisation with the clock signal on CLK.

6.1 Answer-to-Reset in asynchronous transmission

6.1.1 Bit duration

The nominal bit duration used on I/O is defined as one Elementary Time Unit (etu).

For cards having internal clock, the initial etu is $\frac{1}{9\,600}$ s.

For cards using the external clock, there is a linear relationship between the Elementary Time Unit used on I/O and the period provided by the interface device on CLK.

The initial etu is $\frac{372}{f_i}$ s where f_i is in hertz.

See also 6.1.4.1.

The initial frequency f_i is provided by the interface device on CLK during the answer to reset, as defined in 4.2.5.

In order to read the initial character (TS), all cards shall initially be operated with f_i in the range of 1 MHz to 5 MHz.

6.1.2 Character frame during answer to reset

Prior to the transmission of a character, I/O shall be in state Z.

A character consists of ten consecutive bits : a start bit in state A, eight bits of information, designated ba to bh and conveying a data byte, and a tenth bit bi used for even parity checking.

A data byte consists of 8 bits designated b1 to b8, from the least significant bit (lsb, b1) to the most significant bit (msb, b8).

Conventions (level coding, connecting levels Z/A to digits 1 or 0 ; and bit significance, connecting ba—bh to b1—b8) are specified in the initial character, called TS, which is transmitted by the card in response to reset.

Parity is correct when the number of ONES is even in the sequence from ba to bi.

Within a character, the time from the leading edge of the start bit to the trailing edge of the nth bit shall equal (n±0,2) etu.

When searching for a start, the receiver samples I/O periodically. The time origin being the mean between last observation of level Z and first observation of level A, the start shall be verified before 0,7 etu, and then ba is received at (1,5±0,2) etu, bb at (2,5±0,2) etu, ... bi at (9,5±0,2) etu. Parity is checked on the fly.

NOTE — When searching for a start, the sampling time shall be less than 0,2 etu so that all the test zones are distinct from the transition zones.

The delay between two consecutive characters (between start leading edges) is at least 12 etu, including a character duration (10±0,2) etu plus a guardtime. While in guardtime, the interface device and the card remain both in reception, so that I/O is in state Z. See figure 3.

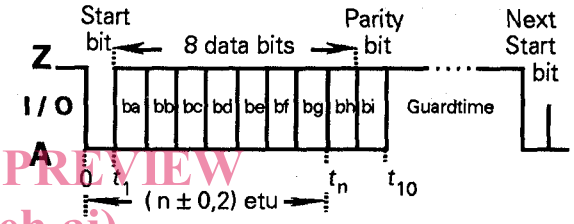


Figure 3 — Character frame

During the answer to reset, the delay between the start leading edges of two consecutive characters from the card shall not exceed 9 600 etu. This maximum value is named initial waiting time.

6.1.3 Error detection and character repetition

During the answer to reset, the following character repetition procedure depends on the protocol type. See 6.1.4.3. This procedure is mandatory for cards using the protocol type T=0 ; it is optional for the interface device and for other cards.

The transmitter tests I/O, (11±0,2) etu after the start leading edge :

— If I/O is in state Z, the correct reception is assumed.

— If I/O is in state A, the transmission is assumed to have been incorrect. The disputed character shall be repeated after a delay of at least 2 etu after detection of the error signal.

When parity is incorrect, from (10,5±0,2) etu, the receiver transmits an error signal as state A for 1 etu minimum and 2 etu maximum. The receiver then shall expect a repetition of the disputed character. See figure 8.

If no character repetition is provided by the card,

— the card ignores and shall not suffer damage from the error signal coming from the interface device ;

— the interface device shall be able to initiate the repetition of the whole Answer-to-Reset sequence.