SLOVENSKI STANDARD

SIST EN 60749-29:2004

julij 2004

Semiconductor devices - Mechanical and climatic test methods - Part 29: Latch-up test (IEC 60749-29:2003)

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ICS 31.080.01

Referenčna številka
SIST EN 60749-29:2004(en)

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EUROPEAN STANDARD

NORME EUROPÉENNE

EUROPÄISCHE NORM

EN 60749-29

December 2003

ICS 31.080

English version

Semiconductor devices – Mechanical and climatic test methods Part 29: Latch-up test (IEC 60749-29:2003)

Dispositifs à semiconducteurs –
Méthodes d'essais mécaniques
et climatiques
Partie 29: Essai de verrouillage
(CEI 60749-29:2003)

Halbleiterbauelemente –
Mechanische und klimatische
Prüfverfahren
Teil 29: Latch-up-Prüfung
(IEC 60749-29:2003)

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European Committee for Electrotechnical Standardization
Comité Européen de Normalisation Electrotechnique
Europäisches Komitee für Elektrotechnische Normung

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Ref. No. EN 60749-29:2003 E

Foreword

The text of document 47/1713/FDIS, future edition 1 of IEC 60749-29, prepared by IEC TC 47, Semiconductor devices, was submitted to the IEC-CENELEC parallel vote and was approved by CENELEC as EN 60749-29 on 2003-12-01.

The following dates were fixed:

– latest date by which the EN has to be implemented at national level by publication of an identical national standard or by endorsement	(dop)	2004-03-01
– latest date by which the national standards conflicting with the EN have to be withdrawn	(dow)	2006-12-01

Endorsement notice

The text of the International Standard IEC 60749-29:2003 was approved by CENELEC as a European Standard without any modification.

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NORME INTERNATIONALE

INTERNATIONAL STANDARD

CEI
IEC
60749-29

Première édition
First edition
2003-11

Dispositifs à semiconducteurs – Méthodes d'essais mécaniques et climatiques –

Partie 29: Essai de verrouillage

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Part 29: Latch-up test

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International Electrotechnical Commission, 3, rue de Varembé, PO Box 131, CH-1211 Geneva 20, Switzerland
Telephone: +41 22 919 02 11 Telefax: +41 22 919 03 00 E-mail: inmail@iec.ch Web: www.iec.ch

Commission Electrotechnique Internationale
International Electrotechnical Commission
Международная Электротехническая Комиссия

CODE PRIX
PRICE CODE S

Pour prix, voir catalogue en vigueur
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SEMICONDUCTOR DEVICES –
MECHANICAL AND CLIMATIC TEST METHODS –

Part 29: Latch-up test

FOREWORD

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International Standard IEC 60749-29 has been prepared by IEC technical committee 47: Semiconductor devices.

This standard cancels and replaces IEC/PAS 62181 published in 2000. This first edition constitutes a technical revision.

The text of this standard is based on the following documents:

FDIS	Report on voting
47/1713/FDIS	47/1724/RVD

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

The committee has decided that the contents of this publication will remain unchanged until 2007. At this date, the publication will be

- reconfirmed;
- withdrawn;
- replaced by a revised edition, or
- amended.

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SEMICONDUCTOR DEVICES – MECHANICAL AND CLIMATIC TEST METHODS –

Part 29: Latch-up test

1 Scope and object

This part of IEC 60749 covers the I-test and the overvoltage latch-up testing of integrated circuits.

This test is classified as destructive.

The purpose of this test is to establish a method for determining integrated circuit (IC) latch-up characteristics and to define latch-up failure criteria. Latch-up characteristics are used in determining product reliability and minimizing "No Trouble Found" (NTF) and "Electrical Overstress" (EOS) failures due to latch-up.

This test method is primarily applicable to CMOS devices. Applicability to other technologies must be established.

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In this part of IEC 60749 latch-up is not related to a specific mechanism but is an electrical failure characteristic that occurs when a device is subjected to this test method.

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The classification of latch-up as a function of temperature is defined in 2.1 and the failure level criteria are defined in 2.10.

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2 Terms and definitions

For the purposes of this document, the following terms and definitions apply.

2.1
classification
the classification defines the latch-up test temperature. Latch-up testing classifications are defined as follows:

Class I – Latch-up testing performed at room temperature.

Class II – Latch-up testing performed at the maximum ambient rated temperature for the device.

If no classification is specified, Class I testing shall be performed.

NOTE Elevated temperature will reduce latch-up resistance and Class II testing is recommended for devices that are required to operate at elevated temperature.

2.2
cool-down time
period of time between successive applications of trigger pulses or the period of time between the removal of the V_{supply} voltage and the application of the next trigger pulse (See Figures 4, 5, and 6 and Table 2.)

2.3
DUT
device under test

2.4
GND (ground)
common or zero-potential pin(s) of the DUT

NOTE 1 Ground pins are not latch-up tested.

NOTE 2 A ground pin is sometimes called V_{ss}.

2.5
input pins
all address, data-in control, V_{ref} and similar pins

2.6
I/O (bi-directional) pins
device pins that can be made to operate as an input or output or in a high-impedance state

2.7
I_{supply}
total supply current in each V_{supply} pin (or pin group) with the DUT biased as indicated in Table 1

2.8
I-test
latch-up test that supplies positive and negative current pulses to the pin under test

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2.9
latch-up
state in which a low-impedance path, resulting from an overstress that triggers a parasitic thyristor structure, persists after removal or cessation of the triggering condition

NOTE 1 The overstress can be a voltage or current surge, an excessive rate of change of current or voltage, or any other abnormal condition that causes the parasitic thyristor structure to become regenerative.

NOTE 2 Latch-up will not damage the device provided that the current through the low-impedance path is sufficiently limited in magnitude or duration.

2.10
level
defines the failure criteria used during latch-up testing. Latch-up failure grades are defined as follows:

Level A – The failure criteria as defined in Table 1

Level B – Special failure criteria. Supplier should provide definition of failure criteria used

2.11
logic-high
level within the more positive (less negative) of the two ranges of logic levels chosen to represent the logic states

NOTE 1 For digital devices, a voltage level equal to V_{supply} is used for latch-up testing, except where otherwise specified in the relevant specification.

NOTE 2 For non-digital devices, V_{supply} voltage level or the maximum operating voltage that can be applied to that pin as defined in the relevant specification may be used for latch-up testing.

2.12
logic-low
level within the more negative (less positive) of the two ranges of logic levels chosen to represent the logic states

NOTE 1 For digital devices, ground voltage level is used for latch-up testing, except where specified in the relevant specification.

NOTE 2 For non-digital devices, ground voltage level or the minimum operating voltage that can be applied to that pin as defined in the relevant specification may be used for latch-up testing.

2.13
maximum V_{supply}
maximum operating voltage for operation within performance specifications

NOTE 1 The maximum voltage ***is not the absolute maximum voltage beyond which permanent damage is likely***.

NOTE 2 Maximum refers to the magnitude of V_{supply} and can be either positive or negative.

2.14
no connect pin
pin that has no internal connection and that can be used as a support for external wiring without disturbing the function of the device

NOTE All “no connect” pins should be left in an open (floating) state during latch-up testing.

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2.15
nominal I_{supply} (I_{nom})
measured dc supply current for each V_{supply} pin (or pin group) with the DUT biased at the test temperature as defined in Clause 4 and Table 1

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2.16
output pin
device pin that generates a signal or voltage level as a normal function during the normal operation of the device

NOTE Output pins, though left in an open (floating) state during testing of other pin types, are latch-up tested.

2.17
preconditioned pin
device pin that has been placed in a defined state or condition (input, output, high impedance, etc.) by applying control vectors to the DUT

2.18
testing of dynamic devices
latch-up trigger testing of a device in a known stable state, at the minimum-rated clock frequency applied to the device (see 4.2.3 for specified conditions)

2.19
test condition
test temperature, supply voltage, current limits, voltage limits, clock frequency, input bias voltages, and preconditioning vectors applied to the DUT during the latch-up test