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INTERNATIONAL STANDARD

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colour inside

Fibre optic communication subsystem test procedures – Part 2-3: Digital systems – Jitter and wander measurements

Procédures d'essai des sous-systèmes de télécommunications à fibres optiques – Partie 2-3: Systèmes numériques – Mesures des gigues et des dérapages

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FOREWORD

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This bilingual version, published in 2010-02, corresponds to the English version.

The text of this standard is based on the following documents:

FDIS	Report on voting
86C/885/FDIS	86C/905/RVD

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

The French version of this standard has not been voted upon.

A list of all parts of the IEC 61280-2 series, published under the general title *Fibre optic communication subsystem test procedures – Digital systems,* can be found on the IEC website.

The committee has decided that the contents of this publication will remain unchanged until the maintenance result date indicated on the IEC web site under "http://webstore.iec.ch" in the data related to the specific publication. At this date, the publication will be

- reconfirmed;
- withdrawn;
- replaced by a revised edition, or
- amended.

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FIBRE OPTIC COMMUNICATION SUBSYSTEM TEST PROCEDURES –

Part 2-3: Digital systems – Jitter and wander measurements

1 Scope

This part of IEC 61280 specifies methods for the measurement of the jitter and wander parameters associated with the transmission and handling of digital signals.

1.1 Types of jitter measurements

This standard covers the measurement of the following types of jitter parameters:

a) jitter tolerance
   1) sinusoidal method
   2) stressed eye method
b) jitter transfer function
c) output jitter
d) systematic jitter
e) jitter separation

1.2 Types of wander measurements

This standard covers the measurement of the following types of wander parameters:

a) non-synchronized wander
b) TDEV tolerance
c) TDEV transfer
d) synchronized wander

2 Normative references

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60825-1, Safety *of laser products – Part 1: Equipment classification and requirements*

ITU-T Recommendation G.813, *Timing characteristics of SDH equipment slave clocks (SEC)*

3 Terms and definitions

For the purposes of this document, the following terms and definitions apply.

NOTE See also IEC 61931.

3.1
jitter
the short-term, non-cumulative, variation in time of the significant instances of a digital signal from their ideal position in time. Short-term variations in this context are jitter components with a repetition frequency equal to or exceeding 10 Hz

3.2
jitter amplitude
the deviation of the significant instance of a digital signal from its ideal position in time

NOTE For the purposes of this standard the jitter amplitude is expressed in terms of the unit interval (UI). It is recognized that jitter amplitude may also be expressed in units of time.

3.3
unit interval
UI
the shortest interval between two equivalent instances in ideal positions in time. In practice this is equivalent to the ideal timing period of the digital signal

3.4
jitter frequency
the rate of variation in time of the significant instances of a digital signal relative to their ideal position in time. Jitter frequency is expressed in Hertz (Hz)

3.5
jitter bandwidth
the jitter frequency at which the jitter amplitude has decreased by 3dB relative to its maximum value

3.6
alignment jitter
jitter created when the timing of a data signal is recovered from the signal itself

3.7
timing jitter
jitter present on a timing source

3.8
systematic jitter
jitter components which are not random and have a predictable rate of occurrence. Systematic jitter in a digital signal results from regularly recurring features in the digital signal, such as frame alignment data, and justification control data. This is sometimes referred to as deterministic jitter and is composed of periodic uncorrelated jitter and data dependent jitter

3.9
periodic uncorrelated jitter
a form of systematic jitter that occurs at a regular rate, but is uncorrelated to the data when the data pattern repeats. Periodic uncorrelated jitter will be the same independent of which edge in a pattern is observed over time. Sources of periodic uncorrelated jitter include switching power supplies phase modulating reference clocks or any form of periodic phase modulation of clocks that control data rates

3.10
inter-symbol interference jitter
caused by bandwidth limitations in transmission channels. If the channel bandwidth is low, signal transitions may not reach full amplitude before transitioning to a different logic state. Starting at a level closer to the midpoint between logic states, the time at which the signal edge then crosses a specific amplitude threshold can be early compared to consecutive identical digits which have reached full amplitude and then switch to the other logic state

3.11
duty cycle distortion
occurs when the duration of a logic 1 (0-1-0) is different from the duration of a logic 0 (1-0-1). For example, if the logic 1 has a longer duration, rising edges will occur early relative to falling edges, compared to their ideal locations in time

3.12
data dependent jitter
represents jitter that is correlated to specific bits in a repeating data pattern. That is, when a data pattern repeats, the jitter on any given signal edge will manifest itself in the same way for any repetition of the pattern. It is due to either duty cycle distortion and/or inter-symbol interference

3.13
waiting time jitter
applies to plesiochronous multiplexing and is defined as the jitter caused by the varying delay between the demand for justification and its execution

3.14
jitter tolerance
maximum jitter amplitude that a digital receiver can accept for a given penalty or alternatively without the addition of a given number of errors to the digital signal. The maximum jitter amplitude tolerated is generally dependent on the frequency of the jitter

3.15
jitter generation
process of adding jitter impairment to a data signal

3.16
input jitter
magnitude of the jitter occurring at a hierarchical interface or the input port of equipment or a device

3.17
output jitter
magnitude of the jitter occurring at a hierarchical interface or the output port of equipment or a device

3.18
jitter transfer
amount of jitter transferred from the input to the output of an equipment or device. It is usually expressed as a ratio (in dB) of the output jitter to the input jitter

3.19
total jitter
the summation (or convolution) of deterministic and random jitter. Total jitter is expressed as a peak value

3.20
jitter bathtub curve
display of bit-error-ratio as a function of the time location of the BERT error detector sampling point. The resulting curve is then a display of the probability that a data edge will be misplaced at or beyond a specific location (closer to the centre of a bit) within a unit interval

3.21
wander
long-term, non-cumulative, variation in time of the significant instances of a digital signal from their ideal position in time. Long-term variations in this context are jitter components with a repetition frequency less than 10 Hz

NOTE For the purpose of this document, the wander amplitude is expressed in units of time (s). It is recognised that wander amplitude may also be expressed in terms of unit interval (UI).

3.22
time interval error
TIE
difference between the measure of a time interval as provided by a clock and the measure of that same time interval as provided by a reference clock. Mathematically, the time interval error function TIE ($t;\tau$) can be expressed as:

$$TIE(t;\tau) = [T(t+\tau) - T(t)] - [Tref(t+\tau) - Tref(t)] = x(t+\tau) - x(t) \qquad (1)$$

where τ is the time interval, usually called observation interval

3.23
maximum time interval error
MTIE
maximum peak-to-peak delay variation of a given timing signal with respect to an ideal timing signal within an observation time ($\tau = n\tau_0$) for all observation times of that length within the measurement period (T). It is estimated using the following formula:

$$MTIE(n\tau_0) \cong \max_{1 \le k \le N-n} \left[\max_{k \le i \le k+n} x_i - \min_{k \le i \le k+n} x_i \right] \qquad n = 1,2 \ldots N-1 \qquad (2)$$

3.24
time deviation
TDEV or σx
measure of the expected time variation of a signal as a function of integration time. TDEV can also provide information about the spectral content of the phase (or time) noise of a signal. TDEV is in units of time. Based on the sequence of time error samples, TDEV is estimated using the following calculation:

$$TDEV(n\tau_0) \cong \sqrt{\frac{1}{6n^2(N-3n+1)} \sum_{j=1}^{N-3n+1} \left[\sum_{i=j}^{n+j-1} (x_{i+2n} - 2x_{i+n} + x_i) \right]^2} \qquad n = 1,2 \ldots, \text{int} \quad part\left(\frac{N}{3}\right) \qquad (3)$$

where

x_i denotes time error samples;

N denotes the total number of samples;

τ_0 denotes the time error-sampling interval;

τ denotes the integration time, the independent variable of TDEV;

n denotes the number of sampling intervals within the integration time t.

3.25
bit error ratio
BER
number of bits received in error as a ratio of the total number of bits received

3.26
errored second
time of 1 s duration that contains one or more digital errors in a data stream

4 General considerations

4.1 Jitter generation

Jitter in a digital signal is generated by three basic processes which are briefly described below. The mathematical analysis of the jitter processes is complex and not within the scope of this standard. A comprehensive analysis and early mathematical treatise of the jitter processes is provided by [1][1].

4.1.1 Timing jitter

Jitter impairment of the original data timing clock. Even the most stable timing sources contain a certain amount of jitter, or unintended phase modulation or phase noise. In primary timing generators this impairment is exceedingly small, but is increased when such timing signals are distributed in a system. The effect of noise on the timing signal in a digital system is demonstrated in an exaggerated degree in Figure 1.

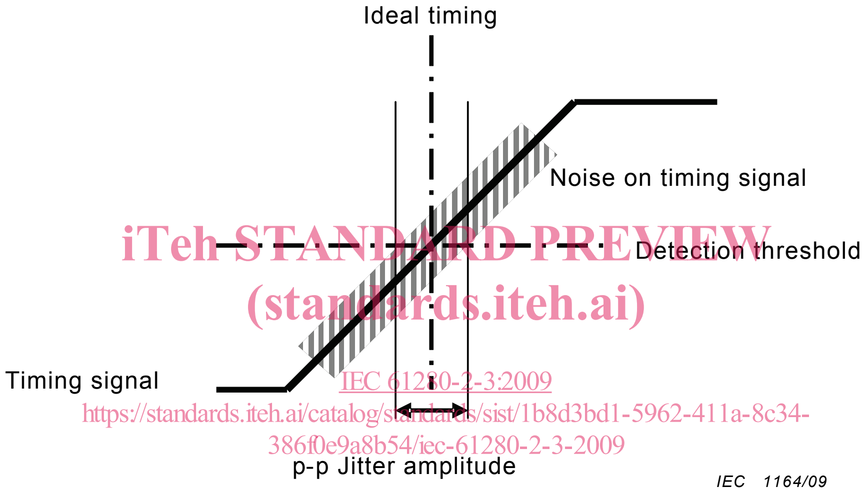


Figure 1 – Jitter generation

4.1.2 Alignment jitter

When a digital pattern is presented to a timing recovery circuit, the continuous variation of the digital pattern results in the creation of jitter in the recovered clock signal relative to the incoming data (alignment jitter). This effect, first analyzed and described in detail by [2] is the major cause of jitter generation. It means that the jitter components of the recovered clock signal are added to the data when they are retimed. The jitter bandwidth created by this process is the same as the analogue bandwidth of the clock recovery circuit used.

When the process is repeated at a similar equipment, the resultant clock signal shows increased jitter due to the addition of timing and alignment jitter. Thus, jitter is added to the data signal, and amplified at the next timing recovery operation. A repetition of this process, such as occurs in transmission links with many repeaters, or chains of add-drop multiplexers, can build up substantial jitter amplitudes; but as long as the bandwidth of the timing recovery process is the same or greater than the jitter bandwidth of the signal, the jitter will always be accommodated. An analysis of the accumulation of jitter in successive timing recovery operations was first published by [3]. The jitter buildup can be represented by an equation of the form:

1 Figures in square brackets refer to the Bibliography.

$$\theta_n = \sum_{k=1}^{n} \theta_0(j\omega)\left(\frac{1}{1+j\omega/B}\right)^k \qquad (4)$$

The above equation yields a jitter power density spectrum which can be expressed in the form:

$$\phi_n \approx n^2 \left[\frac{\sin \frac{n}{2B}\omega}{\frac{n}{2B}\omega}\right]^2 \phi_0 \text{ for } \omega \ll B) \qquad (5)$$

where

θ_n denotes the jitter amplitude after *n* timing recovery processes;

θ_0 denotes the jitter amplitude introduced at each individual timing recovery process;

n denotes the number of tandem timing recovery processes;

ω denotes the angular frequency (2πf) of the jitter component;

B denotes the half angular bandwidth of the timing recovery circuit;

Φ_n denotes the jitter power density after n timing recovery processes;

Φ_0 denotes the jitter power density introduced at each individual timing recovery process.

It should be noted that for low values of frequency the power density and hence amplitude of the jitter increases linearly with the number of tandem timing recovery processes.

In point-to-point communications systems, where transmitter timing is not derived from incoming data, alignment jitter and jitter build-up is not a significant problem.

4.1.3 Other effects

In the course of the transmission of a digital signal, further impairments such as added noise and dispersion effects provide additional jitter components when timing is recovered from the signal. Such effects are more severe when analogue amplification is used rather than digital regeneration in order to increase the length of a digital link.

4.2 Effects of jitter on signal quality

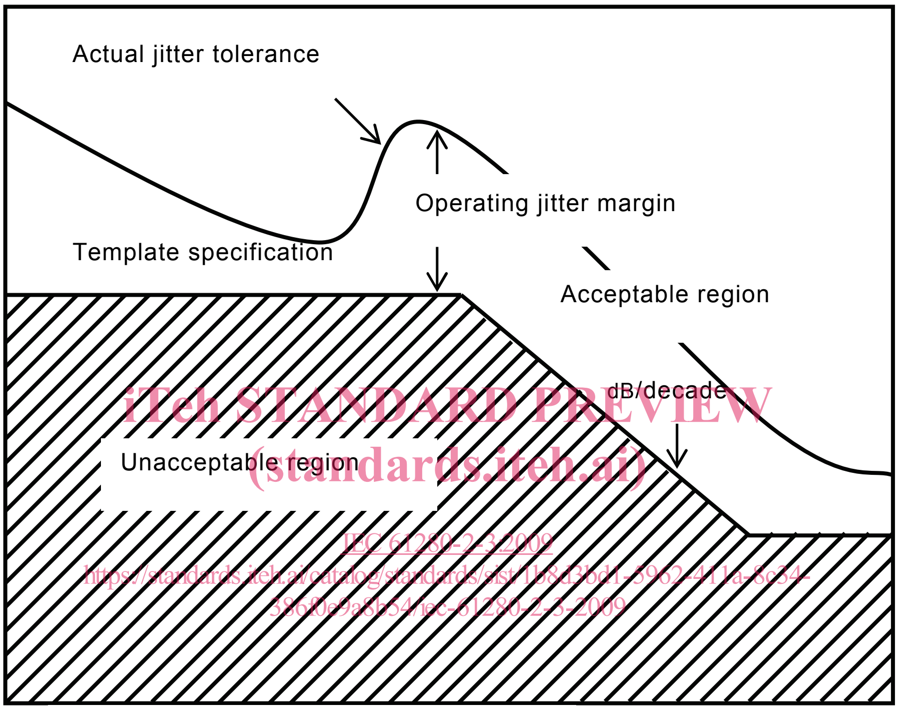
Jitter has no effect on the transmission of data as long as the equipment can accommodate the jitter amplitude and rate of deviation (see 4.3). When jitter is large enough or fast enough such that the receiver decision point is made near or beyond a data edge, a mistake can be made and BER degraded. Jitter, depending on its amplitude and frequency, can also have serious effects on analogue services such as music and television which have been transmitted over digital links. The effect of jitter is to introduce unwanted frequency and phase modulation products which are audible in music and visible on television pictures.

4.3 Jitter tolerance

In telecommunications systems, jitter tolerance requirements are typically specified in terms of jitter templates, which cover a specified sinusoidal amplitude/frequency region. Jitter templates represent the minimum amount of jitter the equipment shall be able to accept without producing the specified degradation of error performance. A typical relationship between actual jitter tolerance and its associated tolerance template is illustrated in Figure 2.

The jitter amplitudes that equipment actually tolerates at a given frequency are defined as all amplitudes up to, but not including, that which causes the designated degradation of error performance. The designated degradation of error performance may be expressed in terms of either bit-error-ratio (BER) penalty or the onset of errors criteria. The existence of these two criteria arises because the input jitter tolerance of digital equipment is primarily determined by the following three factors:

a) ability of the input clock recovery circuit to accurately recover the timing from a jittered data signal, including the presence of other degradations such as pulse distortion, crosstalk, noise, and other impairments;
b) ability of the input circuit buffer, for example an elastic store, to accommodate the jitter amplitude;
c) ability of other components to accommodate dynamically varying input data rates such as pulse justification capacity and synchronizer and de-synchronizer buffer size in an asynchronous digital multiplex.



IEC 1165/09

Figure 2 – Example of jitter tolerance

In data communications systems, jitter tolerance is often determined with signal impairments that are more complex than simple sinusoidal jitter. The general concept is to verify that the receiver is capable of achieving the desired BER when presented with the allowable signal it will encounter in a real system. Thus the jitter tolerance test signal will include impairments that are allowed for both the transmitter and the channel. For example, a real transmitter may have periodic jitter, random jitter, and duty cycle distortion. As the signal traverses the channel, it may be further degraded through a bandwidth limited channel, thus adding inter-symbol interference jitter. As the receiver shall be able to tolerate such a signal in a real system, the signal used to verify receiver tolerance shall include all of these impairments. This method of testing is sometimes referred to as “stressed eye” testing, indicating that the eye diagram of the signal presented to a receiver has been intentionally degraded or stressed.

4.4 Waiting time jitter

When asynchronous (plesiochronous) signals are multiplexed, a justification technique (also known as pulse stuffing) is used which involves the comparison of the phase of the incoming digital signal with the multiplexer’s tributary timing. When a preset difference is detected a control signal is transmitted, via the overhead in the multiplex frame structure, to the demultiplexer. In order to ensure the integrity of the control signal in the presence of errors, it is repeated 3 or 5 times. At the demultiplexer a majority decision is taken to recognize the