

INTERNATIONAL STANDARD

NORME INTERNATIONALE

**Digital addressable lighting interface –
Part 102: General requirements – Control gear**

**Interface d'éclairage adressable numérique –
Partie 102: Exigences générales – Appareillages de commande**

<https://standards.iteh.ai/catalog/standards/sist/14b3caef-5cc6-479d-b509-b74fa01dc927/iec-62386-102-2009>



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3, rue de Varembe
CH-1211 Geneva 20
Switzerland
Email: inmail@iec.ch
Web: www.iec.ch

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CONTENTS

FOREWORD.....	7
INTRODUCTION.....	9
1 Scope.....	10
2 Normative references.....	10
3 Terms and definitions.....	10
4 General.....	12
5 Electrical specification.....	12
6 Interface power supply.....	12
7 Transmission protocol structure.....	12
7.1 General.....	12
7.2 Forward frame.....	12
7.2.1 Address byte 'YAAA AAAS'.....	12
7.2.2 Data byte 'XXXX XXXX'.....	13
7.3 Backward frame.....	13
8 Timing.....	13
8.1 Information bit timing.....	13
8.2 Forward frame timing.....	14
8.3 Backward frame timing.....	15
8.4 Frame sequence timing.....	15
9 Method of operation.....	16
9.1 Logarithmic dimming curve, arc power levels and accuracy.....	16
9.2 Power-on.....	19
9.3 Interface-failure.....	19
9.4 Min and max level.....	19
9.5 Fade time and fade rate.....	20
9.6 Reaction to commands during error state.....	20
9.7 Behaviour during lamp preheating and lamp ignition time.....	21
9.8 Memory access and memory map.....	21
9.8.1 Memory access commands.....	21
9.8.2 Memory map.....	21
10 Declaration of variables.....	24
11 Definition of commands.....	25
11.1 Arc power control commands.....	25
11.1.1 Direct arc power control command:.....	25
11.1.2 Indirect arc power control commands.....	26
11.2 Configuration commands:.....	28
11.2.1 General configuration commands:.....	28
11.2.2 Arc power parameters settings:.....	28
11.2.3 System parameters settings.....	30
11.3 Query commands.....	30
11.3.1 Queries related to status information.....	30
11.3.2 Queries related to arc power parameter settings.....	32
11.3.3 Queries related to system parameter settings.....	32
11.3.4 Application extended commands.....	33
11.4 Special Commands.....	33

11.4.1	Terminate special processes	33
11.4.2	Download information to the DTR	34
11.4.3	Addressing commands	34
11.4.4	Extended special commands	35
11.5	Summary of the command set	38
12	Test procedures	40
12.0	General	40
12.1	Test sequences 'Physical operational parameters'	44
12.1.1	Test sequences 'Waveform'	44
12.1.2	Test sequence 'Frame structure timing'	53
12.1.3	Insulation test	54
12.1.4	Optional test sequences	54
12.1.5	Test sequence 'Response time'	56
12.2	Test sequences 'Configuration commands'	57
12.2.1	Test sequences 'General configuration commands'	57
12.2.2	Test sequences 'Arc power parameter settings'	70
12.2.3	Test sequences 'System parameter settings'	80
12.2.4	Test sequences 'Memory Access'	84
12.3	Test sequences 'Arc power control commands'	88
12.3.1	Test sequences 'Timing'	88
12.3.2	Test sequences 'Dimming curve'	90
12.3.3	Test sequences 'Arc power commands'	95
12.4	Test sequence 'Physical address allocation'	105
12.5	Test sequences 'Random address allocation'	106
12.5.1	Test sequences 'INITIALISE / TERMINATE'	106
12.5.2	Test sequences 'RANDOMISE'	112
12.5.3	Test sequences 'COMPARE / WITHDRAW'	115
12.5.4	Test sequences 'PROGRAM / VERIFY / QUERY SHORT ADDRESS'	118
12.6	Test sequences 'Queries and reserved commands'	124
12.6.1	Test sequences 'Queries'	124
12.6.2	Test sequences 'Reserved commands'	131
Annex A (informative)	Examples of algorithms	136
Annex B (normative)	List of device types	138
Bibliography	139
Figure 1	– Bi-phase coded "1"	14
Figure 2	– Symbols for bi-phase levels: "1";"0"	14
Figure 3	– Forward frame	14
Figure 4	– Forward frame timing	15
Figure 5	– Backward frame	15
Figure 6	– Backward frame timing	15
Figure 7	– Example of frame sequence timing	16
Figure 8	– Transition from forward to backward frames	16
Figure 9	– Transition from backward to forward and from forward to forward frames	16
Figure 10	– The logarithmic dimming curve with a minimum arc power of 0,1 %	17
Figure 11	– Configuration commands timing	28
Figure 12	– General test structure	40

Figure 13 – Activation state and test state	41
Figure 14 – Test sequence 'Current rating'.....	45
Figure 15 – Test sequence 'Voltage rating'	46
Figure 16 – Test sequence 'Back channel rise time / fall time'.....	47
Figure 17 – Test sequence 'Transmission rate'	48
Figure 18 – Test sequence 'Pulse width'	50
Figure 19 – 'Code violation'.....	51
Figure 20 – Waveforms for test 'Code violation':	52
Figure 21 – Test sequence 'Frame structure timing'	53
Figure 22 – Test sequence 'Polarity'	54
Figure 23 – Test sequence 'Overvoltage protection'.....	55
Figure 24 – Test sequence 'Response time'.....	56
Figure 25 – Test sequence 'RESET'.....	57
Figure 26 – Test sequence 'RESET: timeout / command in-between'.....	59
Figure 27 – Test sequence '100 ms-timeout'.....	60
Figure 28 – Test sequence 'Commands in-between'.....	62
Figure 29 – Test sequence 'QUERY VERSION NUMBER'.....	64
Figure 30 – Test sequence 'STORE ACTUAL LEVEL IN THE DTR'.....	65
Figure 31 – Test sequence 'Persistent memory'.....	66
Figure 32 – Test sequence 'DTR1'.....	68
Figure 33 – Test sequence 'DTR2'.....	69
Figure 34 – Test sequence 'STORE THE DTR AS MAX LEVEL'	70
Figure 35 – Test sequence 'STORE THE DTR AS MIN LEVEL'	71
Figure 36 – Test sequence 'STORE THE DTR AS SYSTEM FAILURE LEVEL'.....	73
Figure 37 – Test sequence 'STORE THE DTR AS POWER ON LEVEL'	75
Figure 38 – Test sequence 'STORE THE DTR AS FADE TIME'.....	77
Figure 39 – Test sequence 'STORE THE DTR AS FADE RATE'.....	78
Figure 40 – Test sequence 'STORE THE DTR AS SCENE' / 'GO TO SCENE'.....	79
Figure 41 – Test sequence 'REMOVE FROM SCENE'.....	80
Figure 42 – Test sequence 'ADD TO GROUP' / 'REMOVE FROM GROUP'	81
Figure 43 – Test sequence 'STORE THE DTR AS SHORT ADDRESS'.....	83
Figure 44 – Test sequence 'Memory Bank 0'.....	84
Figure 45 – Test sequence 'Memory Bank 1'.....	85
Figure 46 – Test sequence 'Other Memory Banks'	86
Figure 47 – Test sequence 'ENABLE WRITE MEMORY'	87
Figure 48 – Test sequence 'FADE TIME'.....	88
Figure 49 – Test sequence 'FADE RATE'.....	89
Figure 50 – Test sequence 'Logarithmic dimming curve'	90
Figure 51 – Test sequence 'Dimming curve: DIRECT ARC POWER CONTROL'.....	91
Figure 52 – Test sequence 'Dimming curve: UP / DOWN'	92
Figure 53 – Test sequence 'Dimming curve: STEP UP / STEP DOWN'.....	93
Figure 54 – Test sequence 'Dimming curve: DAPC SEQUENCE'	94
Figure 55 – Test sequence 'OFF'	95

Figure 56 – Test sequence 'DIRECT ARC POWER CONTROL'	96
Figure 57 – Test sequence 'UP'	97
Figure 58 – Test sequence 'DOWN'	98
Figure 59 – Test sequence 'STEP UP'	99
Figure 60 – Test sequence 'STEP DOWN'	100
Figure 61 – Test sequence 'RECALL MAX LEVEL'	101
Figure 62 – Test sequence 'RECALL MIN LEVEL'	102
Figure 63 – Test sequence 'ON AND STEP UP'	103
Figure 64 – Test sequence 'STEP DOWN AND OFF'	104
Figure 65 – Test sequence 'Physical address allocation'	105
Figure 66 – Test sequence 'INITIALISE: 15 minutes timer'	106
Figure 67 – Test sequence 'TERMINATE'	107
Figure 68 – Test sequence 'INITIALISE: short address'	108
Figure 69 – Test sequence 'INITIALISE: no short address'	109
Figure 70 – Test sequence 'INITIALISE: 100 ms timeout'	110
Figure 71 – Test sequence 'INITIALISE: command in-between'	111
Figure 72 – Test sequence 'RANDOMISE: reset values'	112
Figure 73 – Test sequence 'RANDOMISE: 100 ms timeout'	113
Figure 74 – Test sequence 'RANDOMISE: command in-between'	114
Figure 75 – Test sequence 'COMPARE'	115
Figure 76 – Test sequence 'WITHDRAW'	117
Figure 77 – Test sequence 'PROGRAM SHORT ADDRESS'	119
Figure 78 – Test sequence 'VERIFY SHORT ADDRESS'	120
Figure 79 – Test sequence 'QUERY SHORT ADDRESS'	122
Figure 80 – Test sequence 'SEARCH ADDRESS: reset value'	123
Figure 81 – Test sequence 'QUERY DEVICE TYPE'	124
Figure 82 – Test sequence 'QUERY LAMP FAILURE'	125
Figure 83 – Test sequence 'QUERY LAMP POWER ON'	126
Figure 84 – Test sequence 'QUERY LIMIT ERROR'	127
Figure 85 – Test sequence 'QUERY POWER FAILURE'	128
Figure 86 – Test sequence 'QUERY STATUS: control gear ok'	129
Figure 87 – Test sequence 'QUERY STATUS: fade running'	130
Figure 88 – Test sequence 'RESERVED: standard commands'	131
Figure 89 – Test sequence 'Application extended commands'	132
Figure 90 – Test sequence 'RESERVED: special commands 1'	133
Figure 91 – Test sequence 'RESERVED: special commands 2'	134
Figure 92 – Test sequence 'Not supported device types'	135
Table 1 – The logarithmic dimming curve with a minimum arc power of 0,1 %	18
Table 2 – Fade times and fade rates	20
Table 3 – Memory map of memory bank 0	22
Table 4 – Memory map of memory bank 1	23
Table 5 – Memory map of other memory banks	24

Table 6 – Declaration of variables.....	25
Table 7 – Summary of the command set.....	38
Table 8 – Timing combinations for test sequence 'Pulse width'	49
Table 9 – Parameters for test sequence 'RESET'.....	58
Table 10 – Parameters for test sequence '100 ms-timeout'	61
Table 11 – Parameters for test sequence 'Commands in-between'.....	63
Table 12 – Parameters for test sequence 'Persistent memory'	67
Table 13 – Parameters for test sequence 'DTR1'	68
Table 14 – Parameters for test sequence 'DTR2'	69
Table 15 – Parameters for test sequence 'STORE THE DTR AS MAX LEVEL'	70
Table 16 – Parameters for test sequence 'STORE THE DTR AS MIN LEVEL'.....	71
Table 17 – Parameters for test sequence 'STORE THE DTR AS SYSTEM FAILURE LEVEL'	72
Table 18 – Parameters for test sequence 'STORE THE DTR AS POWER ON LEVEL'.....	74
Table 19 – Parameters for test sequence 'STORE THE DTR AS FADE TIME'	76
Table 20 – Parameters for test sequence 'STORE THE DTR AS FADE TIME'.....	78
Table 21 – Parameters for test sequence 'STORE THE DTR AS FADE TIME'.....	79
Table 22 – Parameters for test sequence 'ADD TO GROUP' / 'REMOVE FROM GROUP'.....	81
Table 23 – Parameters for test sequence 'STORE THE DTR AS SHORT ADDRESS'.....	82
Table 24 – Parameters for test sequence 'ENABLE WRITE MEMORY'.....	87
Table 25 – Parameters for test sequence 'FADE TIME'.....	88
Table 26 – Parameters for test sequence 'FADE RATE'	89
Table 27 – Parameters for test sequence 'Logarithmic dimming curve'.....	90
Table 28 – Parameters for test sequence 'Dimming curve: DAPC SEQUENCE'.....	94
Table 29 – Parameters for test sequence 'DIRECT ARC POWER CONTROL'	96
Table 30 – Parameters for test sequence 'COMPARE'	115
Table 31 – Parameters for test sequence 'COMPARE'	116
Table 32 – Parameters for test sequence 'PROGRAM SHORT ADDRESS'	118
Table 33 – Parameters for test sequence 'QUERY SHORT ADDRESS'.....	121
Table 34 – Parameters for test sequence 'QUERY LIMIT ERROR'	127
Table 35 – Parameters for test sequence 'RESERVED: standard commands'	131
Table 36 – Parameters for test sequence 'RESERVED: special commands 1'	133
Table 37 – Parameters for test sequence 'RESERVED: special commands 2'	134
Table B.1 – List of device types	138

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DIGITAL ADDRESSABLE LIGHTING INTERFACE –**Part 102: General requirements –
Control gear**

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International Standard IEC 62386-102 has been prepared by subcommittee 34C: Auxiliaries for lamps, of IEC technical committee 34: Lamps and related equipment.

This International Standard, together with IEC 62386-101 and IEC 62386-201, replaces Clause E.4, "Control by digital signals", and Annex G, "Test procedures for ballasts with digital control interface according to Clause E.4", of IEC 60929:2006.

The text of this standard is based on the following documents:

FDIS	Report on voting
34C/874/FDIS	34C/883/RVD

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

This Part 102 is intended to be used in conjunction with Part 101, which contains general requirements for the relevant product type (system), and with the appropriate part 2XX (particular requirements for control gear) containing clauses to supplement or modify the corresponding clauses in Parts 101 and 102 in order to provide the relevant requirements for each type of product.

A list of all parts of the IEC 62386 series, under the general title: *Digital addressable lighting interface*, can be found on the IEC website.

The committee has decided that the contents of this publication will remain unchanged until the maintenance result date indicated on the IEC website under <http://webstore.iec.ch> in the data related to the specific publication. At this date, the publication will be

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INTRODUCTION

This first edition of IEC 62386-102 is published in conjunction with IEC 62386-101 and with the various parts that make up the IEC 62386-200 series for control gear. A further number of parts covering control devices (to be published as the general requirements standard IEC 62386-103 and the various parts that make up the IEC 62386-300 series of particular requirements for control devices) is under consideration. The division of IEC 62386 into separately published parts provides for ease of future amendments and revisions. Additional requirements will be added as and when a need for them is recognized.

This International Standard, and the other parts that make up the IEC 62386-100 series, in referring to any of the clauses of IEC 62386-101 or IEC 62386-102, specify the extent to which such a clause is applicable and the order in which the tests are to be performed. The parts also include additional requirements, as necessary. All parts that make up IEC 62386-100 series are self-contained and therefore do not include references to each other.

Where the requirements of any of the clauses of IEC 62386-101 are referred to in this International Standard by the sentence "The requirements of IEC 62386-101, Clause "n" apply", this sentence is to be interpreted as meaning that all requirements of the clause in question of Part 101 apply, except any which are clearly inapplicable to the specific type of control gear.

The standardization of the control interface for control of electronic control gear by digital signals is intended to achieve interoperable multi-vendor operation between electronic control gear and lighting control devices, below the level of building management systems. All numbers used in this International Standard are decimal numbers unless otherwise noted. Hexadecimal numbers are given in the format 0xVV, where VV is the value. Binary numbers are given in the format XXXXXXXXb or in the format XXXX XXXX, where X is 0 or 1; "x" in binary numbers means "don't care".

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DIGITAL ADDRESSABLE LIGHTING INTERFACE –

Part 102: General requirements – Control gear

1 Scope

This International Standard specifies a protocol and methods of test for the control by digital signals of electronic control gear for use on a.c. or d.c. supplies.

NOTE Tests in this standard are type tests. Requirements for testing individual control gear during production are not included.

2 Normative references

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60929:2006, *A.C.-supplied electronic ballasts for tubular fluorescent lamps – performance requirements*

IEC 61347-2-3, *Lamp control gear – Part 2-3: Particular requirements for a.c. supplied electronic ballasts for fluorescent lamps*

IEC 62386-101:2009, *Digital addressable lighting interface – Part 101: General requirements – System*

3 Terms and definitions

For the purposes of this document, the terms and definitions given in Clause 3 of IEC 62386-101 and the following apply.

3.1

arc power

power supplied to the light sources (lamps), responsible for their output

3.2

arc power level

internal value representing the target arc power

3.3

forward frame

sequence of bits used to transmit data from a master to a slave

3.4

short address

kind of address used to address an individual control gear in the system

3.5

group address

kind of address used to address a group of control gear in the system at once

3.6**broadcast**

kind of address used to address all control gear in the system at once

3.7**command**

sequence of bits causing any reaction in the receiver

3.8**backward frame**

sequence of bits used to transmit data from a slave to a master

3.9**frame sequence**

group of consecutive frames

3.10**fade time**

time taken for the light output to change from the actual dim level to the target dim level specified by the received command

3.11**fade rate**

speed of change the light output

3.12**search address**

24 bit number used to identify an individual control gear in the system during initialization

3.13**random address**

24 bit address generated by the control gear during initialization

3.14**scene**

preset light output level that can be configured

3.15**DTR (Data transfer register)**

multipurpose registers used to transmit data from a control device to the control gear and vice versa

3.16**response time**

actual time taken for a control gear to change its output without fading

3.17**reset state**

state in which all configurable parameters of the control gear, as shown in Table 6 (including the actual level) have reset values

3.18**global trade item number – GTIN**

number used for the unique identification of trade items worldwide

NOTE The key is comprised of a GS1 or U.P.C. company prefix followed by an item reference number and a check digit. It is described in the “GS1 General Specifications”, Version 7.0, published by the GS1, Avenue Louise 326; BE-1050 Brussels; Belgium; and GS1, 1009 Lenox Drive, Suite 202, Lawrenceville, New Jersey, 08648 USA.

3.19

data byte

second byte of a forward frame

4 General

The requirements of 4.1 and 4.2 of IEC 62386-101 shall apply.

5 Electrical specification

The requirements of Clause 5 of IEC 62386-101 shall apply.

6 Interface power supply

The requirements of Clause 6 of IEC 62386-101 shall apply, if a power supply is integrated with the control gear.

7 Transmission protocol structure

7.1 General

A forward frame as well as a backward frame shall be analysed in the receiver. In case of code violation, the frame shall be ignored 1,7 ms after the occurrence of a code violation, the control gear shall be ready again for a frame reception.

7.2 Forward frame

A forward frame shall consist of 19 bits, as shown in 8.2:

- 1 start bit: (logical '1', bi-phase code)
- 1 address byte 'YAAA AAAS': (bi-phase code)
- 1 data byte 'XXXX XXXX': (bi-phase code)
- 2 stop bits: (idle line)

7.2.1 Address byte 'YAAA AAAS'

The first byte of a forward frame is called the 'address byte'. Every control gear shall be able to react to a short address, 16 group addresses and broadcast. The following addressing scheme shall be used:

Type of addresses:		address byte:
64 short addresses	0 – 63	0AAA AAAS
16 group addresses	0 – 15	100A AAAS
broadcast		1111 111S
special commands		1010 0000 to 1111 1101

Y: short- or group address/broadcast: Y = "0": short address
 Y = "1": group address or broadcast

A: significant address bit

S: selector bit: S = "0": data byte = direct arc power level
 S = "1": data byte = command

When the address byte contains a short address, group address or broadcast address, the least significant bit (S) is known as the "selector bit". It is used to indicate whether a direct arc power level or a command follows in the data byte.

Special commands, requirements for which are given in 11.4, shall use CCCC CCCC transmitted in the address byte for selecting the command.

7.2.2 Data byte 'XXXX XXXX'

The least significant bit of the address byte in case of a short address, group address or broadcast (selector bit 'S') shall indicate whether the data byte contains a direct arc power level or a command:

S = "0": data byte = direct arc power level (see 11.1.1)

S = "1": data byte = command (see 11.1.2 and the subsequent subclauses)

In the case of special commands the content of the data byte shall be defined with the relevant commands, as given in 11.4.

7.3 Backward frame

A backward frame shall be sent only after the reception of a query command or a write memory command.

A backward frame shall consist of 11 bits, as shown in 8.3:

- 1 start bit: (logical '1', bi-phase code)
- 1 data byte 'XXXX XXXX': (bi-phase code)
- 2 stop bits: (idle line)

Depending on the command the backward frame (= answer) shall be either a 'Yes' / 'No' or 8-bit information:

'Yes': 1111 1111

'No': The control gear shall not react (idle line)

8-bit information: XXXX XXXX

8 Timing

8.1 Information bit timing

The start bit and the information bits shall be bi-phase encoded.

The information rate shall be 1 200 bit/s.

$$T_e = \frac{1}{2 \cdot 1200} \text{ s} = 416.67 \mu\text{s}$$

The timing for a logical "1" shall be as shown in Figure 1.