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**Mechanical standardization of semiconductor devices –
Part 6-17: General rules for the preparation of outline drawings of surface mounted semiconductor device packages – Design guide for stacked packages – Fine-pitch ball grid array and fine-pitch land grid array (P-PFBGA and P-PFLGA)**

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**Normalisation mécanique des dispositifs à semiconducteurs –
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CONTENTS

FOREWORD ... 3
INTRODUCTION ... 5
1 Scope ... 6
2 Normative references ... 6
3 Definitions ... 6
4 Terminal position numbering ... 7
5 Drawings ... 8
6 Dimensions ... 16
6.1 Group 1 ... 16
6.2 Group 2 ... 21
7 Dimension table ... 27

Figure 1 – Individual stackable package, P-FBGA (cavity-up) ... 8
Figure 2 – Individual stackable package, P-FBGA (cavity-down) ... 9
Figure 3 – Individual stackable package, P-FLGA (cavity-up) ... 10
Figure 4 – Stacked package outline, P-PFBGA (cavity-up BGA and cavity-up BGA) ... 11
Figure 5 – Stacked package outline, P-PFBGA (cavity-down BGA and cavity-down BGA) ... 12
Figure 6 – Stacked package outline, P-PFBGA (cavity-down BGA + cavity-up LGA） ... 13
Figure 7 – Stacked package outline, P-PFLGA (cavity-up LGA + cavity-up BGA) ... 14
Figure 8 – Functional gauge ... 15
Figure 9 – Pattern of terminal position area ... 15

Table 1 – Dimensions, Group 1 ... 16
Table 2 – Dimensions Group 2 ... 21
Table 3 – Combination of D, E, M_D, and M_E, e = 0.80mm pitch FBGA and FLGA ... 22
Table 4 – Combination of D, E, M_D, and M_E, e = 0,65mm pitch FBGA and FLGA ... 23
Table 5 – Combination of D, E, M_D, and M_E, e = 0,50mm pitch FBGA and FLGA ... 24
Table 6 – Combination of D, E, M_D, and M_E, e = 0,40mm pitch FBGA an FLGA ... 25
Table 7 – Combination of D, E, M_D, and M_E, e = 0,30mm pitch FLGA ... 26
Table 8 – Dimension table ... 27

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MECHANICAL STANDARDIZATION OF SEMICONDUCTOR DEVICES –

Part 6-17: General rules for the preparation of outline drawings of surface mounted semiconductor device packages – Design guide for stacked packages – Fine-pitch ball grid array and fine-pitch land grid array (P-PFBGA and P-PFLGA)

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International Standard IEC 60191-6-17 has been prepared by subcommittee 47D: Mechanical standardization for semiconductor devices, of IEC technical committee 47: Semiconductor devices.

The text of this standard is based on the following documents:

FDIS	Report on voting
47D/785/FDIS	47D/793/RVD

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

A list of all the parts in the IEC 60191 series, under the general title *Mechanical standardization of semiconductor devices*, can be found on the IEC website.

The committee has decided that the contents of this publication will remain unchanged until the stability date indicated on the IEC web site under "http://webstore.iec.ch" in the data related to the specific publication. At this date, the publication will be

- reconfirmed,
- withdrawn,
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INTRODUCTION

The trend toward downsizing and higher density of portable electronic devices has driven LSI packages into smaller and higher density configurations. The market demand of higher density has led to the development of the package stacking technology that enabled miniaturization and higher functionality. The objective of this design guide is to standardize outlines and to get interchangeability of individual stackable packages.

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Part 6-17: General rules for the preparation of outline drawings of surface mounted semiconductor device packages – Design guide for stacked packages – Fine-pitch ball grid array and fine-pitch land grid array (P-PFBGA and P-PFLGA)

1 Scope

This part of IEC 60191 provides outline drawings and dimensions for stacked packages and individual stackable packages in the form of FBGA or FLGA.

2 Normative references

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document applies.

IEC 60191-6, *Mechanical standardization of semiconductor devices – Part 6: General rules for the preparation of outline drawings of surface mounted semiconductor device package*

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IEC 60191-6-5, *Mechanical standardization of semiconductor devices – Part 6-5: General rules for the preparation of outline drawings of surface mounted semiconductor device packages - Design guide for fine-pitch ball grid array (FBGA)*

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3 Terms and definitions

For the purposes of this document, the terms and definitions given in IEC 60191-6 and the following apply.

3.1
individual stackable package
package with an array of metallic balls or lands on the underside of the package for the purpose of surface-mount on a printed circuit board and an array of footprints (lands) on the upper side of the package for stacking packages

NOTE The individual stackable cavity-up FLGA package is a part of this specification on the premise of stacking a cavity-down FBGA with cavity-up FLGA.

3.2
stacked package
assembly of multiple individual stackable packages in a stacked configuration

NOTE The top package can be a standard FBGA specified in IEC 60191-6-5 without any footprints on the upper side of the package. The stand-off height of this standard package, however, shall follow this design guide.

3.3
mould cap height (A_2)
height of the mould cap which contains wire-bonded die or of the exposed flip chip-bonded die with respect to the upper substrate surface of the package

3.4
distance between the mould cap edge and innermost balls (F)
distance between the mould cap edge of the lower package and the innermost terminals of the upper package of the stacked package

3.5
upper side land grid pitch (e_1)
grid pitch of the footprints (lands) on the upper side of the individual stackable package. They will be interconnected with the terminals of a mating upper package

3.6
parallelism tolerance of the mould cap surface (y_1)
parallelism tolerance of the top mould-cap surface of the stacked package or the individual stackable package with respect to the seating plane (datum S), which is established by contact of the crowns of the balls

NOTE For the stacked package, "y_1" is defined as the parallelism tolerance of the top-component surface with regard to the seating plane of the lowest component.

3.7
coplanarity (y)
flatness tolerance controlling the lowest points of the terminals of the individual stackable package or the stacked package

3.8
diameter of the upper side lands (b_2)
diameter of the upper side lands, which will be bonded to the terminals of the mating upper package

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4 Terminal position numbering

When a package is viewed from the terminal side with the index corner in the bottom left corner position, terminal rows are lettered from bottom to top starting with A, then B, C,,,, AA, AB, etc., while terminal columns are numbered from left to right starting with 1. Terminal positions are designated by a row-column grid system and shown as alphanumeric identification, e.g., A1, B1, or AC34.

The letters I, O, Q, S, X and Z are not used for naming the terminal rows.

5 Drawings

Outline drawings are shown in Figure 1, 2, 3, 4, 5, 6 and 7.

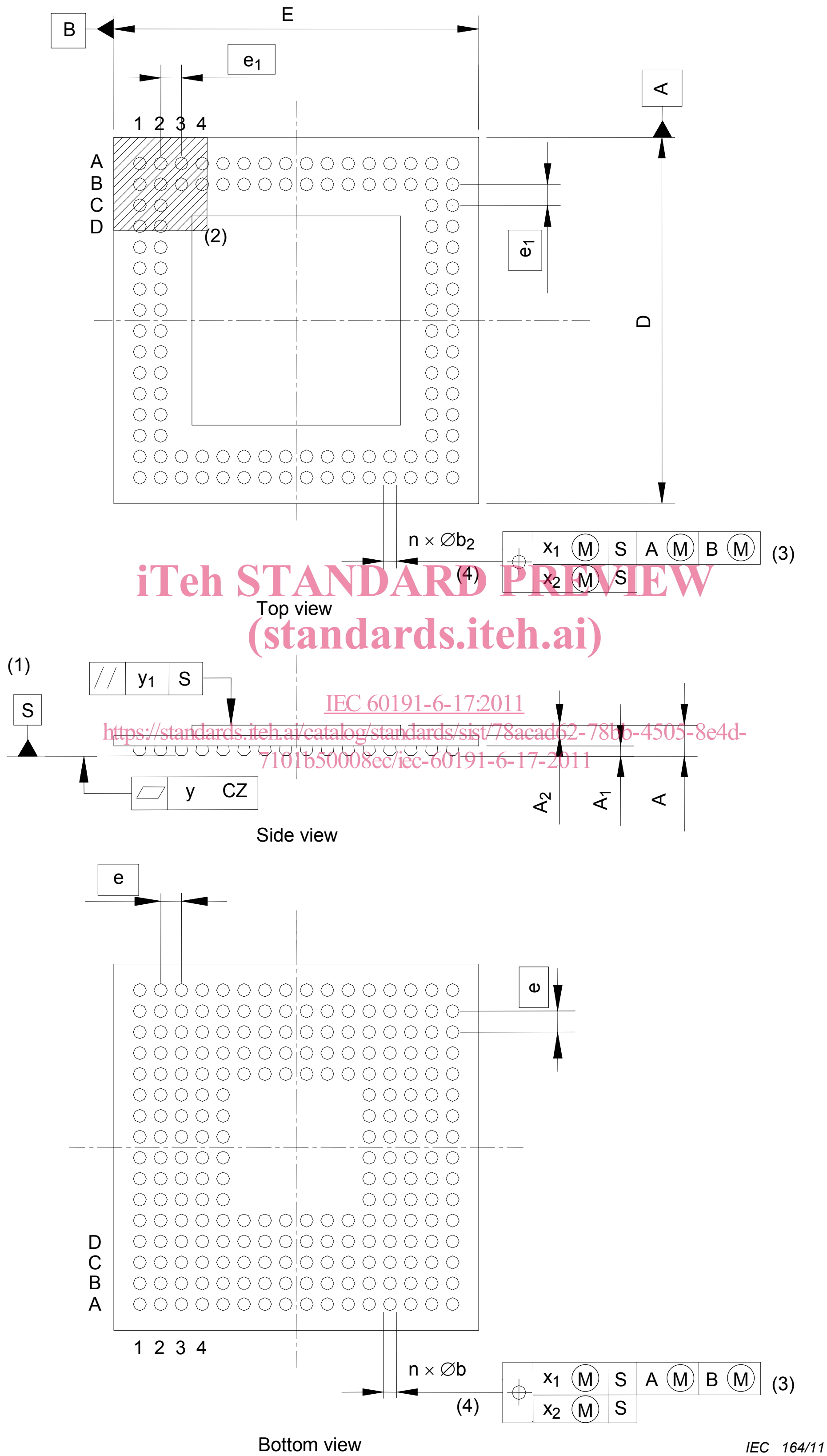

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Figure 1 – Individual stackable package, P-FBGA (cavity-up)

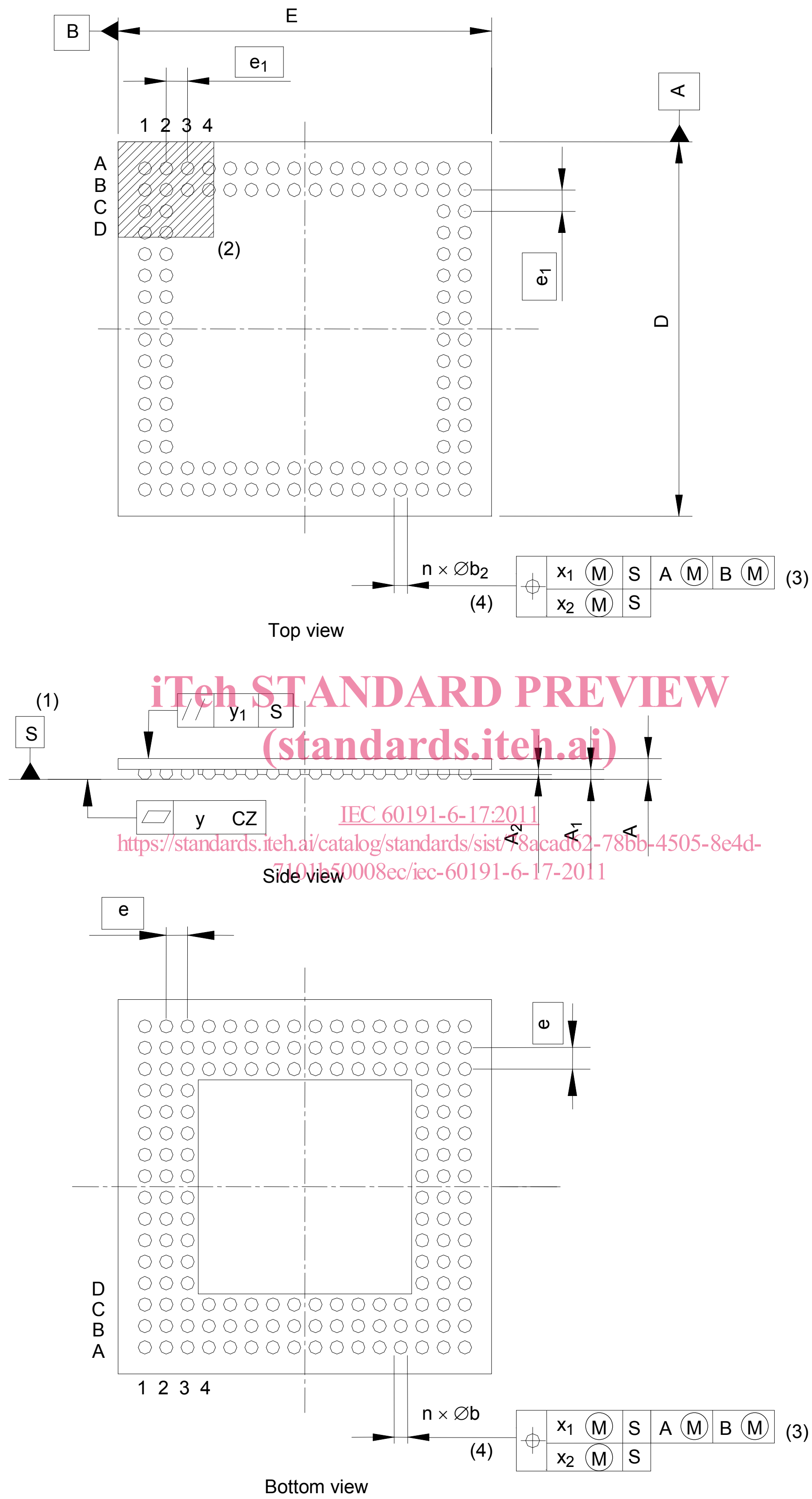

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Figure 2 – Individual stackable package, P-FBGA (cavity-down)

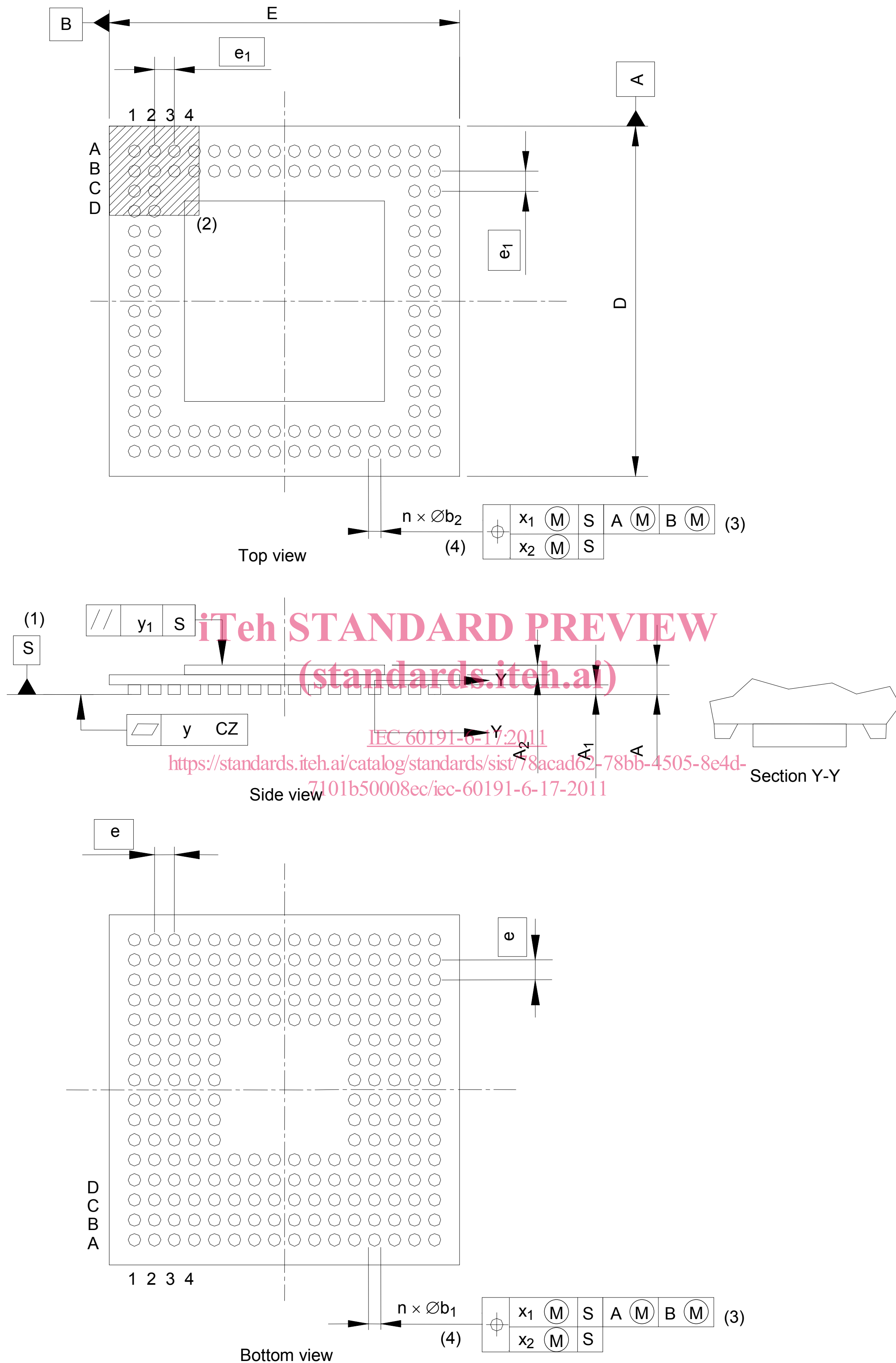

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Figure 3 – Individual stackable package, P-FLGA (cavity-up)

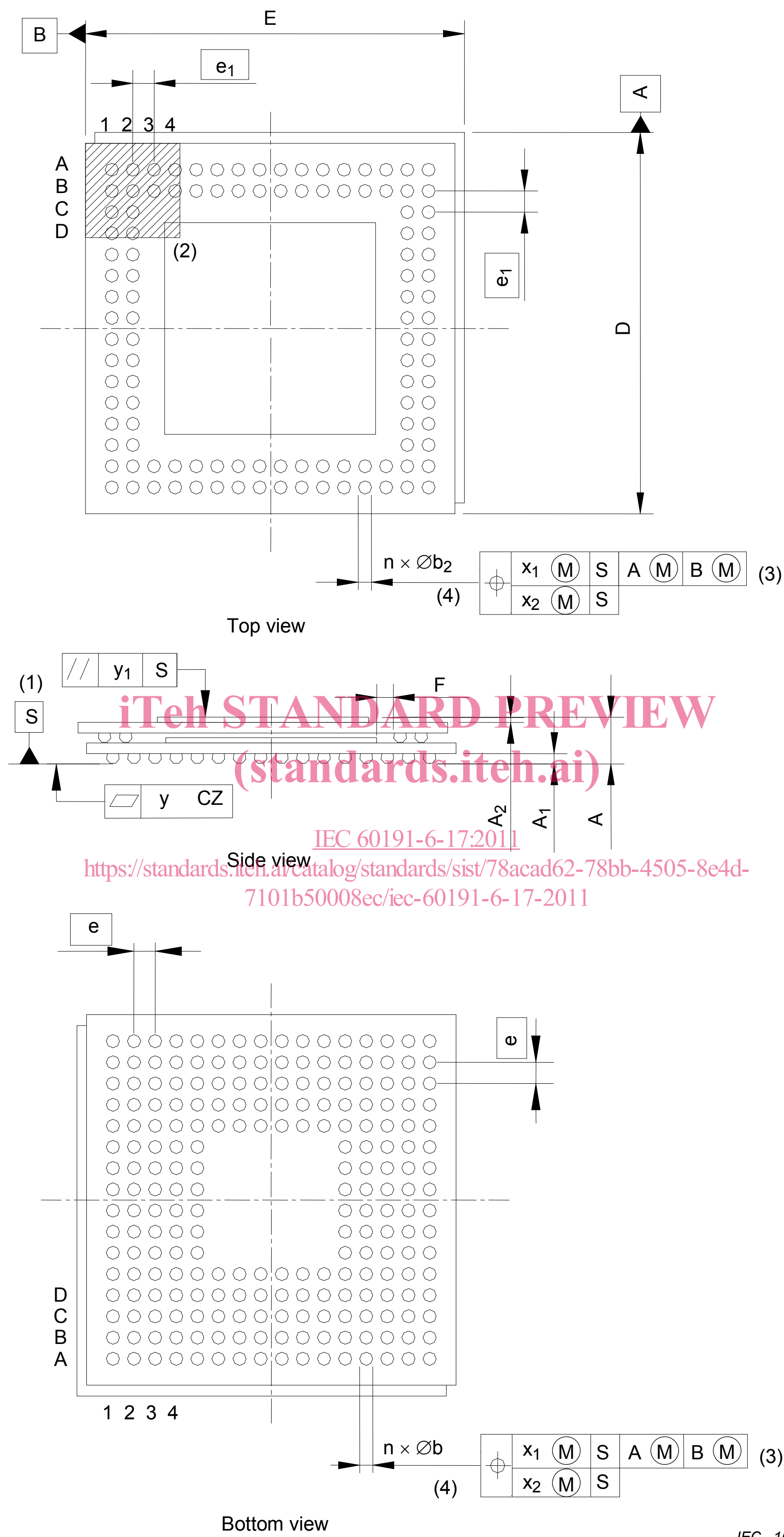

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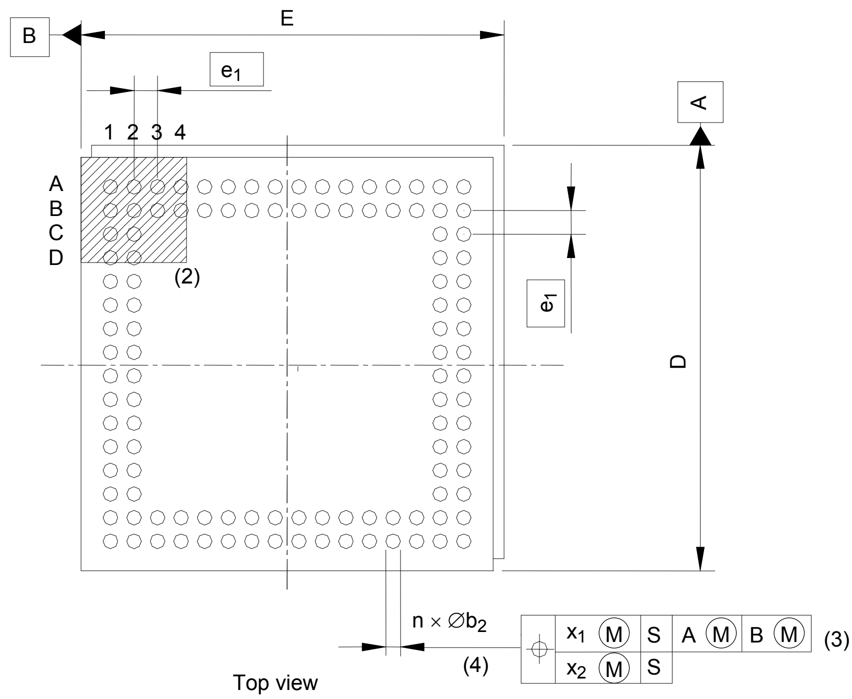
Figure 4 – Stacked package outline, P-PFBGA (cavity-up BGA and cavity-up BGA)



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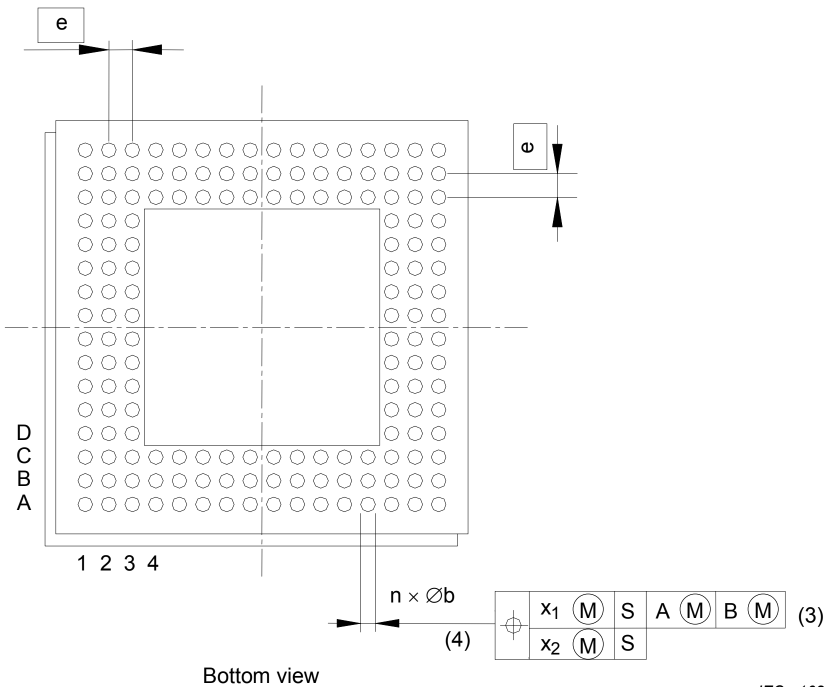

Figure 5 – Stacked package outline, P-PFBGA (cavity-down BGA and cavity-down BGA)

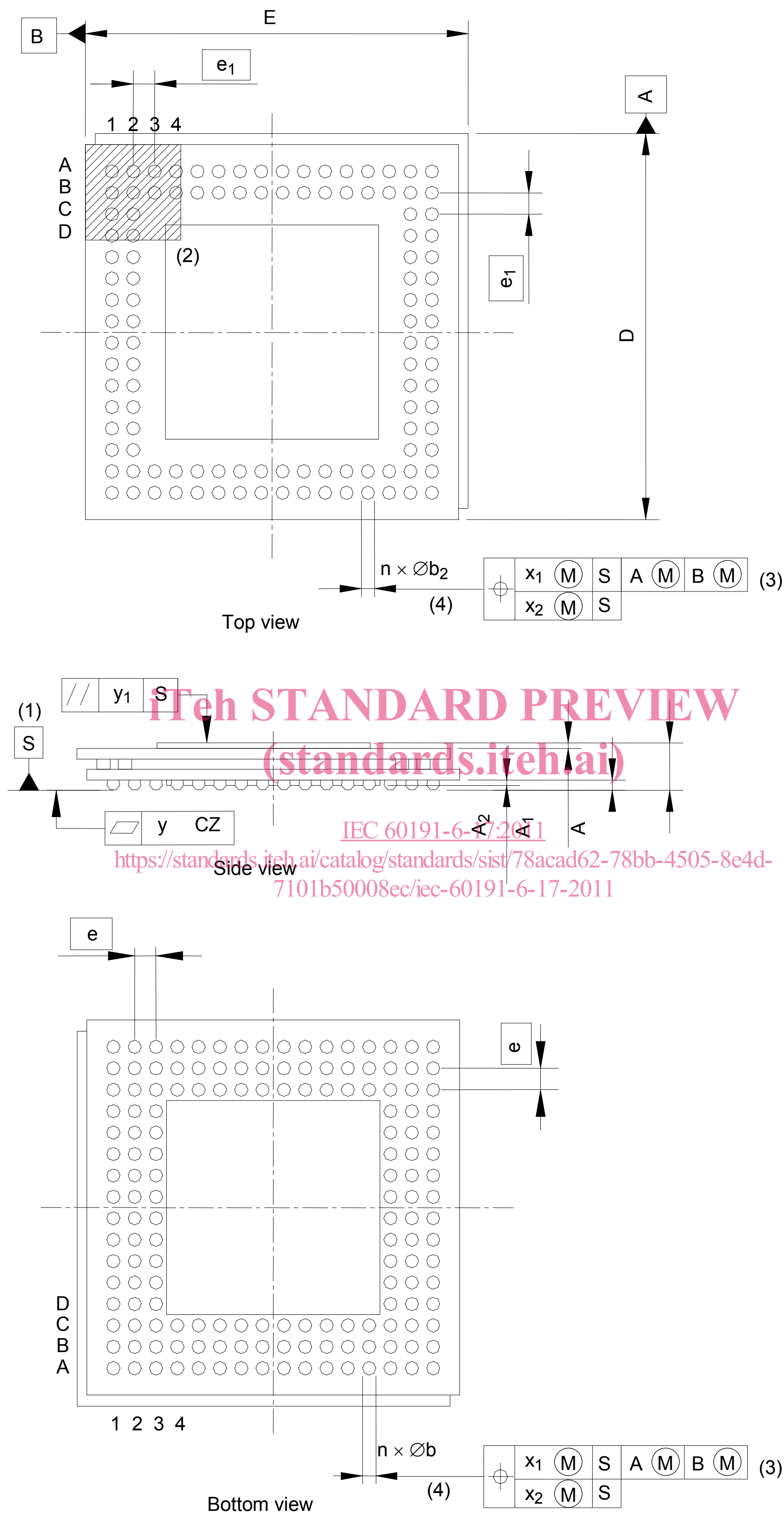

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Figure 6 – Stacked package outline, P-PFBGA (cavity-down BGA + cavity-up LGA)