IEC 61883-1

Edition 3.0 2008-02

INTERNATIONAL STANDARD

Consumer audio/video equipment – Digital interface – Part 1: General

IEC 61883-1:2008(E)

IEC Central Office
3, rue de Varembé
CH-1211 Geneva 20
Switzerland
Email: inmail@iec.ch
Web: www.iec.ch

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INTERNATIONAL ELECTROTECHNICAL COMMISSION

PRICE CODE X

ICS 33.160.01; 35.200

ISBN 2-8318-9610-X

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INTERNATIONAL ELECTROTECHNICAL COMMISSION

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Part 1: General

FOREWORD

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International Standard IEC 61883-1 has been prepared by technical area 4, Digital system interfaces and protocols, of IEC technical committee 100: Audio, video and multimedia systems and equipment.

This third edition of IEC 61883-1 cancels and replaces the second edition, published in 2003, of which it constitutes a technical revision.

The significant technical changes with respect to the second edition are as follows:

– allocation of a new FMT code for the 1394 Trade Association specification '601 over 1394';
– Clarification of the meaning of FMT code;
– harmonization of IEC 61883-1 with IEEE 1394.1 for speeds over S400.

The text of this standard is based on the following documents:

CDV	Report on voting
100/1236/CDV	100/1336/RVC

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

A list of all parts of the IEC 61883 series, under the general title *Consumer audio/video equipment – Digital interface*, can be found on the IEC website.

The committee has decided that the contents of this publication will remain unchanged until the maintenance result date indicated on the IEC web site under "http://webstore.iec.ch" in the data related to the specific publication. At this date, the publication will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

A bilingual version of this publication may be issued at a later date.

CONSUMER AUDIO/VIDEO EQUIPMENT – DIGITAL INTERFACE –

Part 1: General

1 Scope and object

This part of IEC 61883 specifies a digital interface for consumer electronic audio/video equipment using IEEE 1394. It describes the general packet format, data flow management and connection management for audio-visual data, and also the general transmission rules for control commands.

The object of this standard is to define a transmission protocol for audio-visual data and control commands which provides for the interconnection of digital audio and video equipment, using IEEE 1394.

2 Normative references

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEEE 212:2001, *Standard for a Control and Status Registers (CSR) – Architecture for microcomputer buses*

IEEE 1394:1995, *Standard for a High Performance Serial Bus*

IEEE 1394a:2000, *Standard for a High Performance Serial Bus – Amendment 1*

NOTE Throughout this document, the term "IEEE 1394" indicates a reference to the standard that is the result of the editorial combination of IEEE 1394:1995 and IEEE 1394a:2000. Devices conforming solely to IEEE 1394:1995 may conform to IEC 61883. Devices conforming to IEC 61883 should conform to IEEE 1394a:2000.

3 Abbreviations

For the purpose of this document, the following abbreviations apply.

AV/C	Audio Video Control
CHF	CIP Header Field
CIP	Common Isochronous Packet
CMP	Connection Management Procedures
CSR	Command and Status Register
CTS	Command/Transaction Set
CRC	Cyclic Redundancy Check Code
DVCR	Digital Video Cassette Recorder
EOH	End of CIP Header
FCP	Function Control Protocol
iPCR	Input Plug Control Register
iMPR	Input Master Plug Register
MPEG	Motion Picture Experts Group
oPCR	Output Plug Control Register

oMPR Output Master Plug Register
ROM Read Only Memory
spd Speed Encoding
xspd Extended Speed Encoding

For clarity, field names are shown in italics in this standard.

4 High-performance serial bus layers

4.1 Cable physical layer

All cable physical layer implementations conforming to this standard shall meet the performance criteria specified by IEEE 1394. Either the cable and connector defined in IEEE 1394:1995, or the cables and connector defined in IEEE 1394a:2000, shall be used.

When necessary for an AV device to generate a bus reset, it shall follow the requirements of IEEE 1394a:2000, 8.2.1. An AV device that initiates a bus reset should generate an arbitrated (short) bus reset, as specified by IEEE 1394a:2000, in preference to the long bus reset defined by IEEE 1394:1995.

4.2 Link layer

All link layer implementations conforming to this standard shall meet the specifications of IEEE 1394.

4.3 Transaction layer

All transaction layer implementations conforming to this standard shall meet the specifications of IEEE 1394.

5 Minimum node capabilities

A node shall conform to the following requirements.

– A node shall be cycle master capable. This is because every node has the possibility to be assigned as a root.
– A node shall be isochronous resource manager capable, as specified by IEEE 1394:1995, and shall implement the additional isochronous resource manager facilities and responsibilities specified by IEEE 1394a:2000 in 8.3.1.5, 8.3.2.3.8, 8.3.2.3.11, 8.4.2.3 and 8.4.2.6A.
– A node which transmits or receives isochronous packets shall have plug control registers (see 7.2).

5.1 Serial bus management

Bus manager capability is optional for AV devices, but, if implemented by devices conforming to this standard, shall conform to IEEE 1394.

5.2 Command and status registers

5.2.1 CSR core registers

This standard conforms to the CSR architecture. Details of its registers are specified by IEEE 1394.

The STATE_CLEAR.*cmstr* bit shall be implemented as specified by IEEE 1394a:2000, 8.3.2.2.1.

NOTE The *cmstr* bit is set automatically (see IEEE 1394a:2000, 8.3.2.2.1) by system software or hardware when a node becomes the new root after the bus reset process is completed. In this manner, it is possible to ensure the fast resumption and continuity of data transmission where the time scale is critical at the level of microseconds. The rapid activation of a new cycle master decreases the likelihood of a gap in the transmission of cycle start packets; uninterrupted transmission of cycle start packets at nominal 125 µs intervals is critical to the delivery of isochronous data within its latency requirements.

5.2.2 Serial bus node registers

Implementation requirements for bus-dependent registers in this standard conform to IEEE 1394. A node shall have the following registers:

CYCLE_TIME register

BUS_TIME register

BUS_MANAGER_ID register

BANDWIDTH_AVAILABLE register

CHANNELS_AVAILABLE register

A node should have the following register specified by IEEE 1394a:2000:

BROADCAST_CHANNEL register

5.2.3 Configuration ROM requirements

A node shall implement the general ROM format as defined in IEEE 1212:2001 and IEEE 1394. Additional information required for implementations of this standard shall be included in one of the unit directories. Figure 1 shows an example of the configuration ROM implementation for this standard.

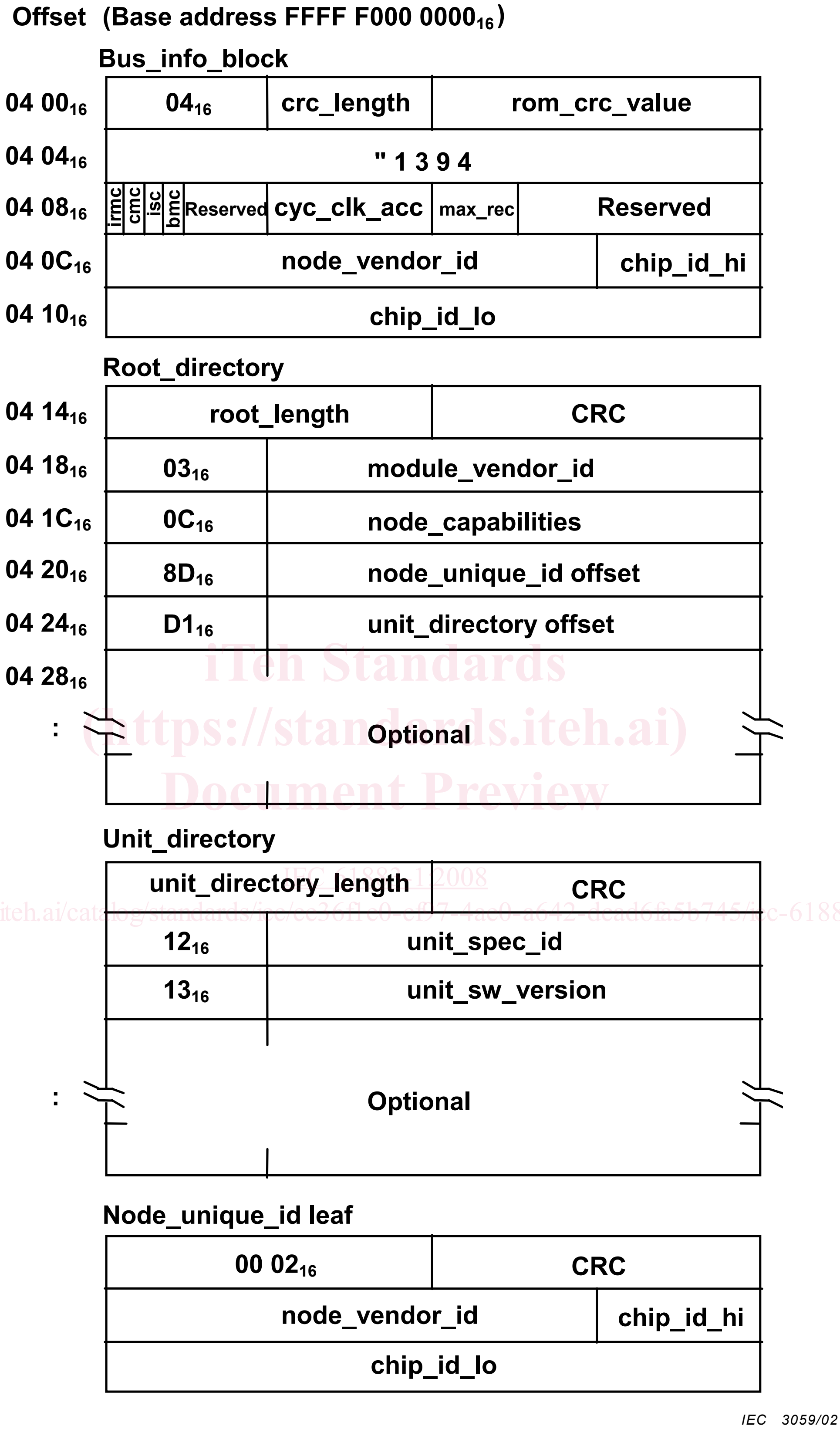

Figure 1 – Configuration ROM