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INTERNATIONAL STANDARD

NORME INTERNATIONALE

colour inside

Semiconductor devices –
Part 1: Time-dependent dielectric breakdown (TDDB) test for inter-metal layers

Dispositifs à semiconducteurs –
Partie 1: Essai de rupture diélectrique en fonction du temps (TDDB) pour les couches intermétalliques

IEC 62374-1:2010

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SEMICONDUCTOR DEVICES –

Part 1: Time-dependent dielectric breakdown (TDDB) test for inter-metal layers

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The text of this standard is based on the following documents:

FDIS	Report on voting
47/2063/FDIS	47/2077/RVD

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

A list of all the parts in the IEC 62374 series, under the general title *Semiconductor devices*, can be found on the IEC website.

The committee has decided that the contents of this publication will remain unchanged until the stability date indicated on the IEC web site under "http://webstore.iec.ch" in the data related to the specific publication. At this date, the publication will be

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SEMICONDUCTOR DEVICES –

Part 1: Time-dependent dielectric breakdown (TDDB) test for inter-metal layers

1 Scope

This part of IEC 62374 describes a test method, test structure and lifetime estimation method of the time-dependent dielectric breakdown (TDDB) test for inter-metal layers applied in semiconductor devices.

2 Terms and definitions

For the purposes of this document, the following terms and definitions apply.

2.1
leakage current of inter-metal layer
I_{leak}
current through the dielectric layer when a use voltage is applied

2.2
initial leakage current of inter-metal layer
I_{leak-0}
leakage current of inter-metal layer before a stress voltage is applied

2.3
compliance current
I_{comp}
maximum current of the voltage-forcing equipment

NOTE A compliance limit can be specified for a particular test.

2.4
measured leakage current of inter-metal layer
I_{meas}
measured current in constant voltage stress (CVS) test

2.5
breakdown time
t_{bd}
summation of time during which stress voltage is applied to inter-metal layer until failure

NOTE In CVS test, applied stress voltage is interrupted by measuring and assessing repeatedly (see Figure 5).

2.6
dielectric layer thickness
t_d
physical thickness of dielectric layer which is pitched between metal lines

2.7
stress voltage
V_{stress}
voltage applied during CVS test

2.8
use voltage
V_{use}
voltage applied during pre-test and used for lifetime estimation

NOTE This voltage is usually power supply voltage.

2.9
metal electrode length
L
total length of metal electrode which is pitching the dielectric layer

2.10
electric field for inter-metal layer
E_{im}
voltage across a dielectric layer divided by its horizontal width between metal lines

NOTE The dielectric layer width should be determined by a consistent documented method by the physical measurement method with SEM, TEM or other. The method or a reference to a documented standard which describes the method should be included in the data report.

3 Test equipment

This TDDB test can be applied by both the package level test and the wafer level test. A high temperature oven is used for the package level test. In the case of the wafer level test, a wafer probe with a hot plate or hot chuck is necessary. Additionally the instruments need to have sufficient resolution to detect changes of leakage current under high temperature condition.

NOTE Package level test is test on test structures assembled in package.

4 Test samples

4.1 General

Test samples for TDDB test for inter-metal layer shall have the following test structure.

4.2 Test structure

An appropriate test structure for this test is an interdigitated one as shown in Figure 1, consisting of comb and serpent patterns, which are connected to the voltage source lines. There is an alternative structure, that is the interdigitated comb and comb structure shown in Figure 2. Test structure leads shall be designed to prevent unexpected failures outside the test structure during the TDDB test. Patterns with vias (Figures 3 and 4) need to be considered because the failure mechanism might be different from a line-to-line pattern without via. Unless otherwise specified comb and serpent pattern are be recommended. The minimum line-to-line spacing is the most severe condition for this mechanism. Therefore, the minimum dimension allowed by the layout rule shall be evaluated. The total length of the metal line is recommended to be in the range from 0,01 m to 1 m. For the accurate lifetime estimation, it is recommended that at least three device conditions of area or length be used, so proper scaling can be achieved. Unless otherwise specified the above-mentioned conditions shall be used for test structure parameters.

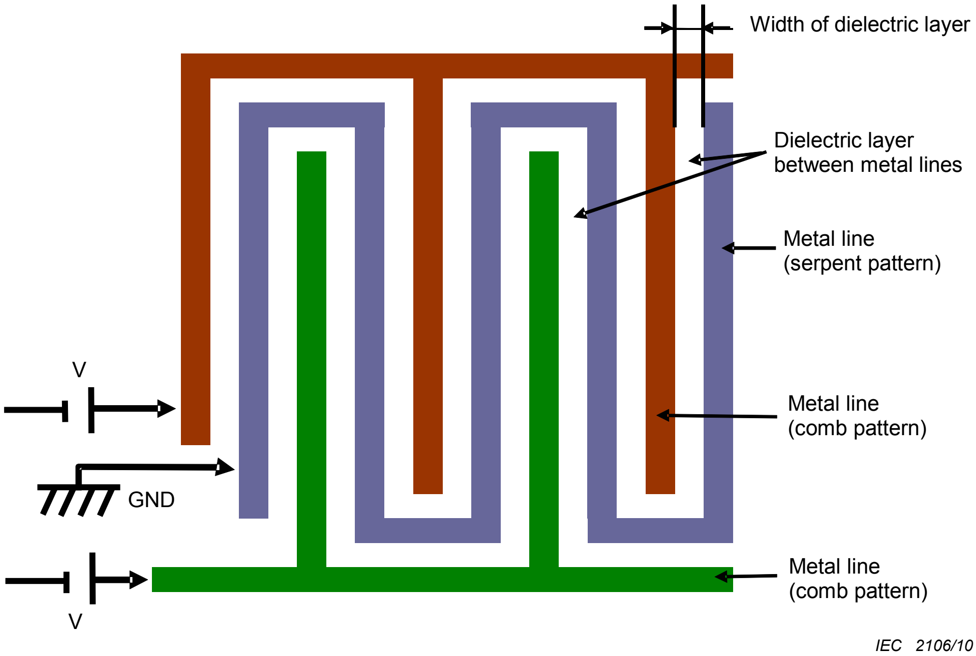


Figure 1 – Schematic image of test structure (comb and serpent pattern)

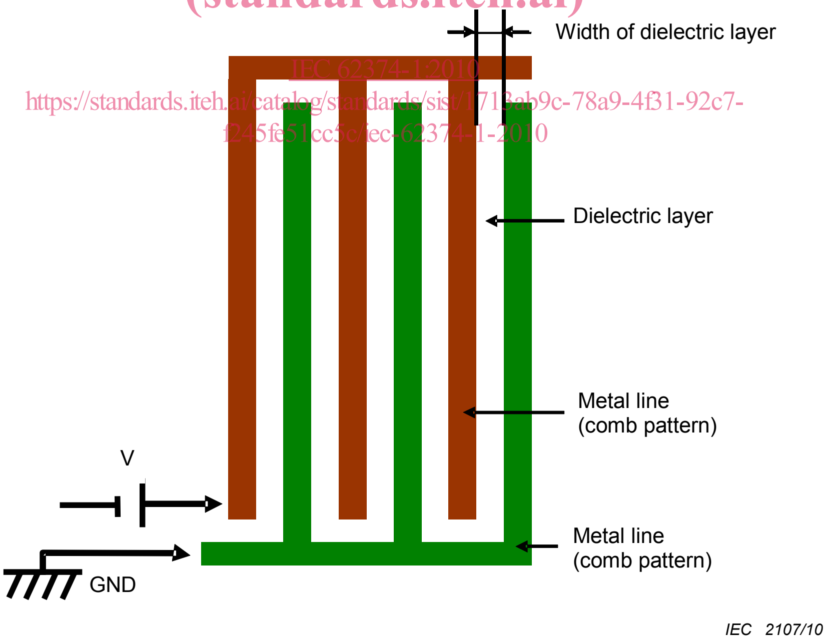


Figure 2 – Schematic image of test structure (comb and comb pattern)

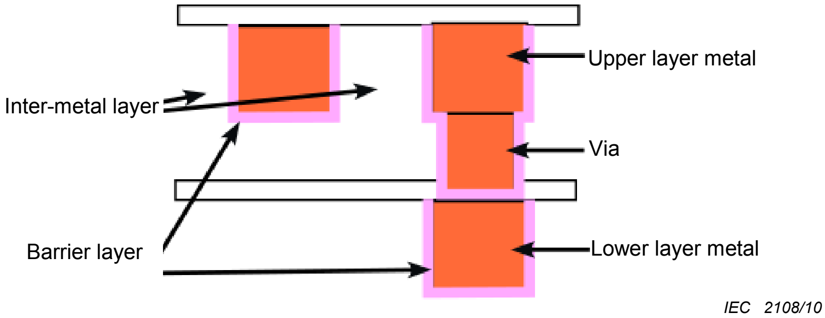


Figure 3 – Cross-sectional image of test structure for line to stacked line including via

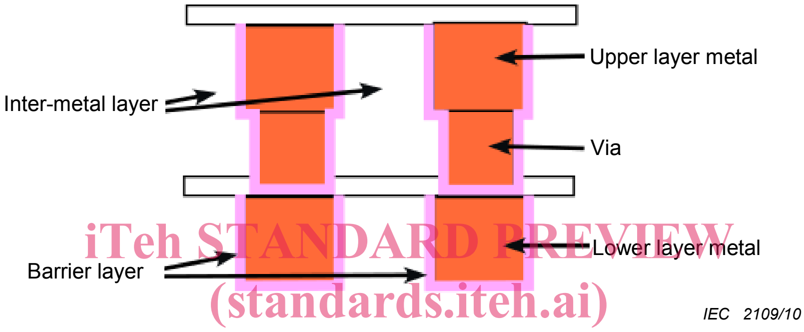


Figure 4 – Cross-sectional image of test structure for stacked line to stacked line including via

5 Procedures

5.1 General

In this section the test procedure is explained. Figure 5 shows a procedure for the constant voltage stress method.

5.2 Pre-test

Pre-test is performed to identify initial failed samples. The leakage current is measured at the applied use voltage. If the measured current is larger than the defined criterion, then that sample is rejected as an initial failed sample. When obtaining the defective distribution as necessary, the CVS test without pre-test may be effective. In this case the pre-test can be omitted.

5.3 Test conditions

5.3.1 General

The following test condition is recommended for the TDDB test. The sample size should be selected to provide the necessary confidence level for the application.

5.3.2 Electric field

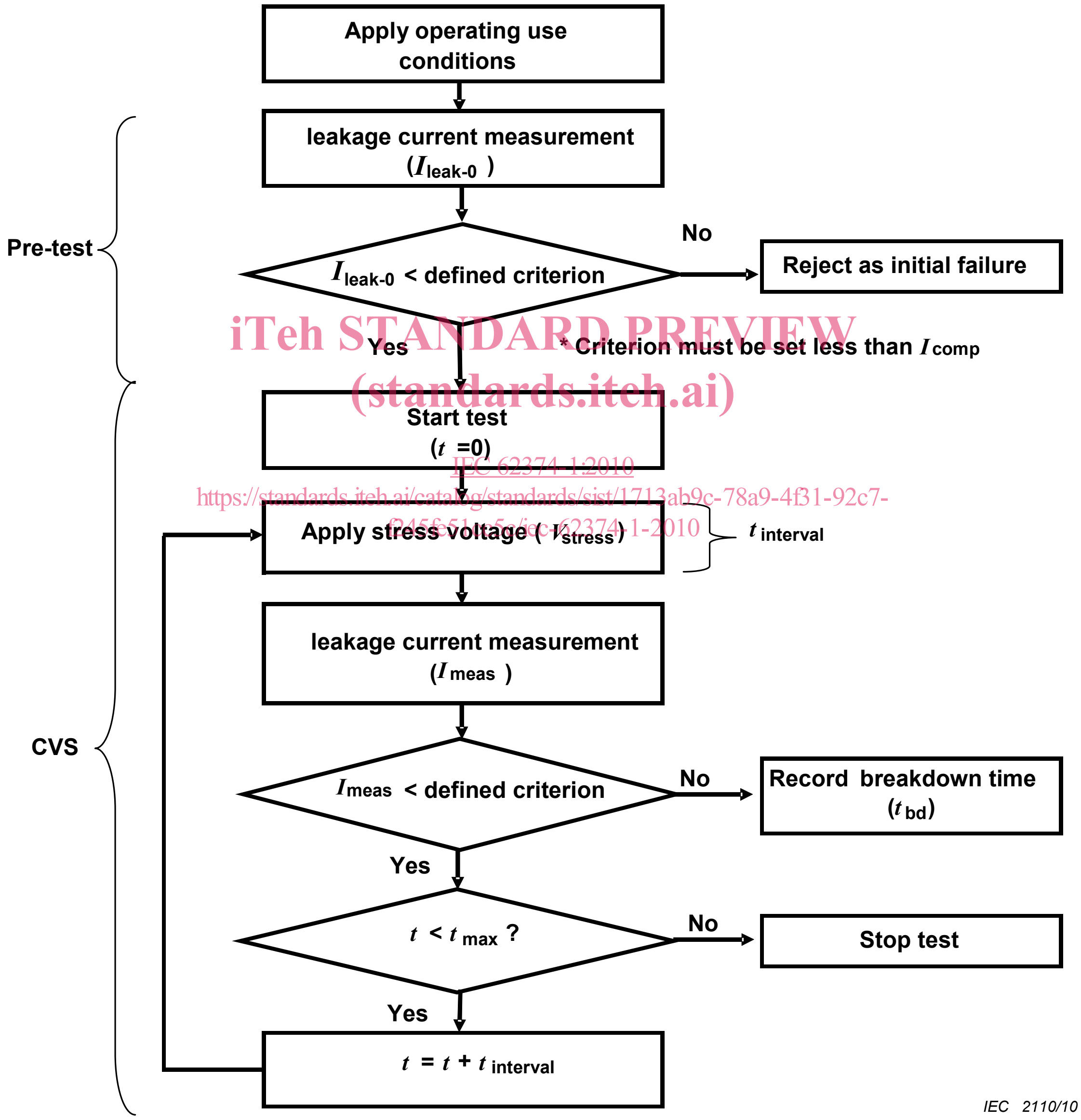
V_{stress} shall be decided by a trial test to get the TDDB lifetime data in a reasonable time. It is preferable to select at least three electric fields for estimating the field acceleration factor.

5.3.3 Temperature

It is preferable to select at least three temperatures. Use-junction temperature shall be in the test temperature range for estimating the temperature acceleration factor (activation energy).

5.4 Failure criterion

Unless otherwise specified, I_{meas} which exceeds the failure criterion indicates device failure. The measurement condition (temperature, electric field) for the pass judgment shall be set up at use conditions or stress conditions. The leakage current shift for failure shall be established in consideration of the initial current, the measurement resolution, and the products specifications.



t, t_{max}, $t_{interval}$ total stress voltage applied time, maximum stress voltage applied time for evaluation, stress voltage applied time of each measurement loop, respectively

Figure 5 – Test flow diagram of constant voltage stress method

6 Lifetime estimation

6.1 General

The method to get the temperature and voltage acceleration factor is explained in this section.

6.2 Acceleration model

The electric field E model is widely used to consider as an acceleration model and it contains the temperature acceleration model (Arrhenius model). Unless otherwise specified in the failure acceleration model, E model should be adopted as the acceleration model for lifetime estimation.

NOTE There were some reports based on the square root-E model recently, and other models' verifications are expected to be published in the future. When a new type of model is adopted, an evaluation to confirm the model adaptability needs to be carried out.

6.3 Formula of E model

$$TTF = A \times \exp\left(\frac{E_a}{kT}\right) \exp\left(-\gamma \times E_{im}\right) \quad (1)$$

where

TTF is the time to failure;

A is the constant;

E_{im} is the electric field for inter-metal layer;

k is the Boltzmann constant;

γ is the electric field acceleration factor;

E_a is the activation energy.

6.4 A procedure for lifetime estimation

a) Make a plot of each stress data point using a Weibull distribution or Log-normal distribution. Unless otherwise specified, Weibull is recommended as the distribution of choice. Refer to [8][1] for an explanation of the Weibull label, left axis cumulative failure rate and bottom axis breakdown time – see Figure 6.

b) Calculate each failure time $t(F\%)$. Next, make a plot of each failure time versus electric field values (E model). Calculate the electric field acceleration factor from the slope (see Figure 7). Then plot each failure versus with the reciprocal of temperature ($1/T$). Calculate the temperature acceleration factor from the slope (activation energy) (see Figure 8).

Using the above acceleration factors, estimate the lifetime $t(F\%)$ at the use condition at certain temperature and voltage.

NOTE 1 For Weibull statistics the correct time to be determined is the time at 63,2% failure. It is the characteristic time of the Weibull distribution and has the largest confidence. In the case of the log-normal distribution the correct time would be the time at 50% failures. So, when the electric field acceleration factor or temperature acceleration factor is calculated, it is preferable that they be calculated with the failure rates which are near that value. The cumulative failure distribution, especially for the Weibull distribution, should be recorded.

NOTE 2 Highly accelerated tests may not provide long enough breakdown times to provide adequate time resolution and may not be enough to determine the correct acceleration model and the correct acceleration factor. Long term test at package level may be required.

[1] The figures in square brackets refer to the Bibliography.