SLOVENSKI STANDARD

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Integrirana vezja – Meritve elektromagnetne odpornosti od 150 kHz do 1 GHz – 5. del: Metoda s Faradayevo kletko (IEC 62132-5:2005)

Integrated circuits - Measurement of electromagnetic immunity, 150 kHz to 1 GHz - Part 5: Workbench Faraday cage method (IEC 62132-5:2005)

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EUROPEAN STANDARD

NORME EUROPÉENNE

EUROPÄISCHE NORM

EN 62132-5

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ICS 31.200

English version

Integrated circuits – Measurement of electromagnetic immunity, 150 kHz to 1 GHz Part 5: Workbench Faraday cage method
(IEC 62132-5:2005)

Circuits intégrés –
Mesure de l'immunité électromagnétique, 150 kHz à 1 GHz
Partie 5: Méthode de la cage de Faraday sur banc de travail
(CEI 62132-5:2005)

Integrierte Schaltungen –
Messung der elektromagnetischen Störfestigkeit im Frequenzbereich von 150 kHz bis 1 GHz
Teil 5: Verfahren mit Faradayschem Arbeitskäfig
(IEC 62132-5:2005)

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CENELEC

European Committee for Electrotechnical Standardization
Comité Européen de Normalisation Electrotechnique
Europäisches Komitee für Elektrotechnische Normung

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Foreword

The text of document 47A/721/FDIS, future edition 1 of IEC 62132-5, prepared by SC 47A, Integrated circuits, of IEC TC 47, Semiconductor devices, was submitted to the IEC-CENELEC parallel vote and was approved by CENELEC as EN 62132-5 on 2005-12-01.

This standard is to be read in conjunction with EN 62132-1.

The following dates were fixed:

– latest date by which the EN has to be implemented at national level by publication of an identical national standard or by endorsement	(dop)	2006-09-01
– latest date by which the national standards conflicting with the EN have to be withdrawn	(dow)	2008-12-01

This European Standard makes reference to International Standards. Where the International Standard referred to has been endorsed as a European Standard or a home-grown European Standard exists, this European Standard shall be applied instead. Pertinent information can be found on the CENELEC web site.

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Première édition
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Circuits intégrés – Mesure de l'immunité électromagnétique, 150 kHz à 1 GHz –

Partie 5: Méthode de la cage de Faraday sur banc de travail

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Integrated circuits – Measurement of electromagnetic immunity, 150 kHz to 1 GHz –

Part 5: Workbench Faraday cage method

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INTERNATIONAL ELECTROTECHNICAL COMMISSION

INTEGRATED CIRCUITS – MEASUREMENT OF ELECTROMAGNETIC IMMUNITY, 150 kHz TO 1 GHz –

Part 5: Workbench Faraday cage method

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International Standard IEC 62132-5 has been prepared by subcommittee 47A: Integrated circuits, of IEC technical committee 47: Semiconductor devices.

The text of this standard is based on the following documents:

FDIS	Report on voting
47A/721/FDIS	47A/728/RVD

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

This standard is to be read in conjunction with IEC 62132-1[1].

IEC 62132 consists of the following parts, under the general title *Integrated circuits – Measurement of electromagnetic immunity, 150 kHz to 1 GHz:*

Part 1: General conditions and definitions

Part 2: Measurement of Radiated Immunity – TEM-Cell and Wideband TEM-Cell Method [2]

Part 3: Bulk Current Injection (BCI), 10 kHz to 1GHz [3]

Part 4: Direct RF power injection method [4]

Part 5: Workbench Faraday cage method

The committee has decided that the contents of this publication will remain unchanged until the maintenance result date indicated on the IEC web site under "http://webstore.iec.ch" in the data related to the specific publication. At this date, the publication will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

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1 To be published.

2 Under consideration.

3 In preparation.

4 To be published.

INTEGRATED CIRCUITS – MEASUREMENT OF ELECTROMAGNETIC IMMUNITY, 150 kHz TO 1 GHz –

Part 5: Workbench Faraday cage method

1 Scope

This measurement procedure describes a measurement method to quantify the RF immunity of integrated circuits (ICs) mounted on a standardized test board or on their final application board (PCB), to electromagnetic conductive disturbances.

2 Normative references

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60050(131): *International Electrotechnical Vocabulary (IEV) – Chapter 131: Electric and magnetic circuits*

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IEC 60050(161): *International Electrotechnical Vocabulary (IEV) – Chapter 161: Electromagnetic compatibility*

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IEC 62132-1: *Integrated circuits – Measurement of electromagnetic immunity, 150 kHz to 1 GHz – Part 1: General conditions and definitions* [5]

IEC 61000-4-6: *Electromagnetic compatibility (EMC) – Part 4: Testing and measurement techniques – Section 6: Immunity to conducted disturbances, induced by radio-frequency fields*

3 Terms and definitions

For the purposes of this document, the definitions of IEC 62132-1, IEC 60050(131) and IEC 60050(161), as well as the following, apply.

3.1
common-mode point
node in a circuit or at a PCB at which a single point is taken as signal terminal, the second terminal being the signal's reference (forming a 2-terminal port). As an example of a common-mode point, the ground reference plane (V_{SS}-plane) at an edge of a PCB is considered with respect to an external reference, e.g. the bottom of the workbench Faraday cage.

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[5] To be published.

3.2
common-mode port
virtual node of a circuit or at a connector port at which the signal follows the vector sum of all signals (including ground) at that port in relation to a reference port. As an example, the bottom of the Workbench Faraday cage is considered an external reference. At a common-mode port with multiple wires, this node can be established by using a passive summation network.

NOTE For a shielded (multi-wire) cable, the screen of that cable is used as common-mode port terminal. In this case, the common-mode point is the screen of that cable.

4 General

4.1 Applicability

This standard applies to ICs that can perform "stand-alone" functions when used on a physically small test board.

The RF immunity of these ICs can be measured under pre-defined conditions. In addition, the method allows measurements on application boards. This gives the user an indication of the expected immunity once the IC(s) is implemented.

This method makes it possible to classify ICs for dedicated functions where EMC constraints are applicable. This might apply to ICs used with cordless telephones, other communication devices and applications where EMC properties are important to obtain optimal operation e.g. automotive, process measurement and control equipment and all other products that control critical functions.

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4.2 Measurement philosophy

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The workbench method is derived from the IEC 61000-4-6. The method described in that publication assumes that supply and signal cable(s) are attached to an electrically small test board, with dimensions ≤ λ/2, i.e. 0,15 m at 1 GHz, see note. These connected cables become the dominant antennas; the induced RF disturbance is injected to the test board via these “antennas”.

NOTE The test board and its connected cables thereto should be partly supported by material with low dielectric constant, as such ε_r = 1 is assumed, see also 7.7.

The connected cables will have functions such as supply, communication and other signal interfaces and these cables are commonly not geometrically oriented in the same plane as the other cables.

The antenna (common-mode) impedance per port has been normalised to 150 Ω with tolerances in the various frequency bands. By injecting either a voltage in series or a current through these common-mode impedances, the RF immunity test is established.

Direct injection of RF disturbance to the IC package is very small, see also IEC 62132-2 as an additional measurement method, and often negligible compared to the disturbance injected through the connected cable(s). Due to the fact that induced currents will flow through the reference of the test board, indirect coupling between the voltages and currents through the package are also established.

Because of the concept chosen, the workbench method shows the effect of the test board layout, the IC supply decoupling, the RF performance of the used discrete components (capacitors, inductors) as well as the measures taken on the IC (e.g. on-chip decoupling, filtered inputs and Schmitt-triggers used, etc.). Similar modes of operation (by software or function) shall be used for the various ICs to be tested to allow comparison. In addition, various modes of operation with one IC allow comparison i.e. determination of contribution of individual blocks within the IC.