IEC 62258-1

Edition 2.0 2009-04

INTERNATIONAL STANDARD

NORME INTERNATIONALE

Semiconductor die products –
Part 1: Procurement and use

Produits de puces de semiconducteurs –
Partie 1: Approvisionnement et utilisation

IEC 62258-1:2009

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SEMICONDUCTOR DIE PRODUCTS –

Part 1: Procurement and use

FOREWORD

1) The International Electrotechnical Commission (IEC) is a worldwide organization for standardization comprising all national electrotechnical committees (IEC National Committees). The object of IEC is to promote international co-operation on all questions concerning standardization in the electrical and electronic fields. To this end and in addition to other activities, IEC publishes International Standards, Technical Specifications, Technical Reports, Publicly Available Specifications (PAS) and Guides (hereafter referred to as "IEC Publication(s)"). Their preparation is entrusted to technical committees; any IEC National Committee interested in the subject dealt with may participate in this preparatory work. International, governmental and non-governmental organizations liaising with the IEC also participate in this preparation. IEC collaborates closely with the International Organization for Standardization (ISO) in accordance with conditions determined by agreement between the two organizations.
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International Standard IEC 62258-1 has been prepared by IEC technical committee 47: Semiconductor devices.

This second edition cancels and replaces the first edition published in 2005, and constitutes a technical revision.

The main changes that have been introduced in this issue have been to ensure consistency across all parts of the standard. The ordering of the subclauses, particularly in Clause 6, has been changed to be more logical and the text of some of the requirements has been amended to add requirements on further information as covered by IEC/TR 62258-4, IEC/TR 62258-7 and IEC/TR 62258-8. New requirements include information on permutability of terminals and functional elements (6.6.4) and moisture sensitivity for partially encapsulated devices (8.8).

The text of this standard is based on the following documents:

CDV	Report on voting
47/1974/CDV	47/2004/RVC

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

A list of all the parts in the IEC 62258 series, under the general title *Semiconductor die products*, can be found on the IEC website.

The committee has decided that the contents of this publication will remain unchanged until the maintenance result date indicated on the IEC web site under "http://webstore.iec.ch" in the data related to the specific publication. At this date, the publication will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

INTRODUCTION

This standard is based on the work carried out in the ESPRIT 4th Framework project GOOD-DIE which resulted in the publication of the ES59008 series of European specifications. Organisations that helped prepare this document included the European IST ENCASIT project, JEITA, JEDEC and ZVEI.

The structure of this International Standard as currently conceived is as follows:

Part 1: Procurement and use

Part 2: Exchange data formats

Part 3: Recommendations for good practice in handling, packing and storage (technical report)

Part 4: Questionnaire for die users and suppliers (technical report)

Part 5: Requirements for information concerning electrical simulation

Part 6: Requirements for information concerning thermal simulation

Part 7: XML schema for data exchange (technical report)

Part 8: EXPRESS model schema for data exchange (technical report)

Further parts may be added as required.

SEMICONDUCTOR DIE PRODUCTS –

Part 1: Procurement and use

1 Scope

This part of IEC 62258 has been developed to facilitate the production, supply and use of semiconductor die products, including

- wafers,
- singulated bare die,
- die and wafers with attached connection structures,
- minimally or partially encapsulated die and wafers.

The standard defines the minimum requirements for the data that are needed to describe such die products and is intended as an aid to the design of and procurement for assemblies incorporating die products. It covers the requirements for data, including

- product identity
- product data
- die mechanical information
- test, quality, assembly and reliability information
- handling, shipping and storage information

It covers the specific requirements for the data that are needed to describe the geometrical properties of die, their physical properties and the means of connection necessary for their use in the development and manufacture of products. It also contains, in the annexes, a vocabulary and list of common acronyms.

2 Normative references

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60050 (all parts), *International Electrotechnical Vocabulary*

IEC 60191 (all parts), *Mechanical standardization of semiconductor devices*

IEC 60191-4:1999, *Mechanical standardization of semiconductor devices – Part 4: Coding system and classification into forms of package outlines for semiconductor device packages*
Amendment 1 (2001)
Amendment 2 (2002)

IEC 61360-1, *Standard data element types with associated classification scheme for electric components – Part 1: Definitions – Principles and methods*

IEC 62258-2, *Semiconductor die products – Part 2: Exchange data formats*

IEC/TR 62258-3, *Semiconductor die products – Part 3: Recommendations for good practice in handling, packing and storage*

IEC/TR 62258-4, *Semiconductor die products – Part 4: Questionnaire for die users and suppliers*

IEC 62258-5, *Semiconductor die products – Part 5: Requirements for information concerning electrical simulation*

IEC 62258-6, *Semiconductor die products – Part 6: Requirements for information concerning thermal simulation*

IEC/TR 62258-7, *Semiconductor die products – Part 7: XML schema for data exchange*

IEC/TR 62258-8, *Semiconductor die products – Part 8: EXPRESS model schema for data exchange*

ISO 14644-1:1999, *Cleanrooms and associated controlled environments – Part 1: Classification of air cleanliness*

3 Terms and definitions

For the purpose of this document, the following terms and definitions are applicable. All the terms and definitions defined here are in addition to the relevant terms and definitions that are defined in IEC 60050 series[1]. Additional terms and acronyms are given for information in Annexes A and B.

3.1 Basic definitions

3.1.1
die (singular or plural)
separated piece(s) of semiconductor wafer that constitute a discrete semiconductor or whole integrated circuit

3.1.2
wafer
slice or flat disc, either of semiconductor material or of such a material deposited on a substrate, in which devices or circuits are simultaneously processed and which may be subsequently separated into die

3.1.3
singulated die
individual and distinct die which have been separated from the wafer

3.1.4
singulation
die separation
separation of wafers into individual die devices, including sawing, scribing and dicing

3.1.5
bare die
unpackaged discrete semiconductor or integrated circuit with pads on the upper surface suitable for interconnection to the substrate or package

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[1] The terms in this series are available at www.Electropedia.org, also known as the "IEV On line".

3.1.6
bare die with connection structures
unpackaged die that have had added bumps, lead frames or other terminations to interconnect for electrical attachment

NOTE Typically these can be die that have had solder or other metallic bumps added to the metallised pads on the die in the form of peripheral bumps or arrays (also known as flip-chip) or die that have had fine leads attached to the metallised pads on the die known as TAB.

3.1.7
minimally-packaged die
MPD
die that have had some exterior packaging medium and interconnection structure added for protection and ease of handling

NOTE This definition includes such packaging technologies as Chip Scale Package (CSP) and Wafer Level Package (WLP) in which the area of the package is not significantly greater than the area of the bare die.

3.1.8
die device
bare die, with or without connection structures, or a minimally-packaged die

3.1.9
data package
aggregate of information on a die device produced in compliance with this standard

3.2 General terminology

3.2.1
chip
common parlance for die

3.2.2
chip scale package
chip size package
CSP
generic term for packaging technologies that result in a packaged part that is only marginally larger than the internal die

3.2.3
wafer level package
WLP
generic term for packaging technologies in which the encapsulation and any interconnection structures are added to the wafer before separation into individual die

3.2.4
discrete (semiconductor)
single two-, three- or four-terminal semiconductor device

NOTE Discrete semiconductors include such devices as individual diodes, transistors and thyristors.

3.2.5
hybrid (circuit)
module or encapsulated sub-assembly that comprises semiconductor die and printed or otherwise attached passive components

NOTE Also see multi-chip module and multi-chip package.

3.2.6
known good die
KGD
qualification of a semiconductor die which indicates that the die has been tested to a specified or determined level of quality or "goodness"

NOTE A commonly accepted definition of KGD is a die that has been tested and/or screened to quality levels that are of the same order as those applicable to the equivalent packaged parts.

3.2.7
package
total assembly which protects one or more electronic components from mechanical, environmental and electrical damage throughout its operational life and which provides means of interconnection

3.2.8
packaging
process of assembling one or more electronic components into a package

NOTE The use of "packaging" as a participle (e.g. "When packaging ICs into dual-in-line packages …") is deprecated.

3.2.9
packing
material which is used to protect electronic items from mechanical, environmental and electrical damage during transportation or storage and which is discarded prior to the incorporation of the item into its end application

3.2.10
multi-chip module
MCM
module that contains two or more die and/or minimally-packaged die

NOTE Also see hybrid 3.2.5 and multi-chip package 3.2.11.

3.2.11
multi-chip package
MCP
package that contains two or more die and/or minimally-packaged die

NOTE Also see hybrid (3.2.5) and multi-chip module (3.2.10).

3.2.12
system in a package
SiP
functional system or sub-system in a single package that contains two or more die devices that individually perform separate system functions

3.2.13
multi-device sub-assembly
MDS
sub-system which consists of multiple electronic devices including at least one integrated circuit

NOTE This is a generic term which includes, among others, hybrid, MCM, MCP and SiP.

3.2.14
pad
conducting feature on a die device forming a terminal to which external electrical connections are made

NOTE For bare die without external connections, the pad acts as the terminal itself. For bumped die the terminal is in the form of additional conducting material placed on a pad whilst for die with attached lead frame the terminal is in the form of a conductor connected to the pad and extending from the die.

3.3 Semiconductor manufacturing and interconnection terminology

3.3.1
mask
a) optical overlay used in photo-etching during the process of semiconductor fabrication

b) major individual patterning stages that are used within the fabrication process

3.3.2
layer
level in the interconnection structure on a die device

3.3.3
passivation
top or final processing and covering on a die, usually of semiconductor oxide or nitride, that protects and seals the active areas of the die from further external chemical or mechanical contamination

NOTE Bond pads require an opening in this passivation to allow electrical contact.

3.3.4
scribe line
scribe lane
area surrounding the die that is set aside on the wafer for the purposes of scribing and sawing the die from the wafer

NOTE This feature may be covered by many other terms such as scribe street, saw lane, dicing lane etc.

3.3.5
wire bonding
process of attaching interconnection wire or ribbon to a die

3.3.6
bond pads
metallised areas on the die that are used for temporary or permanent electrical connection (bonding)

3.3.7
bump
pillar
post
column
raised metallised area on the die that is used for temporary or permanent electrical connection

3.3.8
lead frame
supporting structure upon which a die is mounted and which also includes the connection structure to which the die is bonded

3.3.9
die attach
method and materials used to attach a die to a substrate

3.3.10
flip-chip
semiconductor die which is electrically and/or mechanically connected to an interconnection structure in such a way that the active area faces the interconnection structure

3.3.11
interposer
material placed between two surfaces giving electrical insulation, mechanical strength and/or controlled mechanical separation between the two surfaces

NOTE An interposer may be used as a means for redistributing electrical connections and/or allowing for different thermal expansions between adjacent surfaces.

3.3.12
redistribution
process of moving terminals on die to more convenient positions by additional connectivity layers or by the use of an interposer

3.3.13
die stacking
wafer stacking
placing of die or wafers on top of each other to form a three dimensional stack die stacking

NOTE 1 Die are interconnected by wire-bonding, edge plating or printing, or by using through silicon vias.

NOTE 2 Die or wafers may be stacked back to face and/or face to face.

3.3.14
through silicon via
TSV
interconnection structure made through the semiconductor material of the die device from one surface of the device to the other

NOTE The via may also have a bump, pillar or post attached to either or both sides to enable stacking of the die, or the via itself may form a copper nail.

4 General requirements

Suppliers of die devices shall furnish, in a data package, information that is necessary and sufficient for users of the devices at all stages of design, procurement, manufacture and test of products containing them. Details of the requirements are given below and in other parts of this standard.

Whilst it is expected that much of the information supplied in conformance with this International Standard will be in the public domain and available from such sources as manufacturers' data sheets, this specification does not place an obligation on a supplier to make information public. Any information that a supplier considers to be proprietary or commercially sensitive may be supplied under the terms of a non-disclosure agreement.

For further details of requirements, refer to Clauses 6 to 12.

5 Data exchange

It is recommended that data intended for exchange by electronic means should be formatted in accordance with the provisions of IEC 62258-2, IEC/TR 62258-7 and IEC/TR 62258-8. The questionnaire in IEC/TR 62258-4, and the associated spreadsheet, may be used as an aid to compliance with the requirements of this part of the standard with the possibility of converting the spreadsheet content into one of the exchange formats.