IEC 62525

Edition 1.0 2007-11

INTERNATIONAL STANDARD

IEEE 1450™

Standard Test Interface Language (STIL) for Digital Test Vector Data

IEC 62525:2007(E) IEEE Std. 1450-1999

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Standard Test Interface Language (STIL) for Digital Test Vector Data

INTERNATIONAL ELECTROTECHNICAL COMMISSION

PRICE CODE XG

ICS 25.040;19.080

ISBN 2-8318-9337-2

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INTERNATIONAL ELECTROTECHNICAL COMMISSION

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STANDARD TEST INTERFACE LANGUAGE (STIL) FOR DIGITAL TEST VECTOR DATA

FOREWORD

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The text of this standard is based on the following documents:

IEEE Std	FDIS	Report on voting
1450(1999)	93/247/FDIS	93/258/RVD

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

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IEEE Standard Test Interface Language (STIL) for Digital Test Vector Data

Sponsor

Test Technology Standards Committee of the IEEE Computer Society

Approved 18 March 1999

IEEE-SA Standards Board

Abstract: Standard Test Interface Language (STIL) provides an interface between digital test generation tools and test equipment. A test description language is defined that: (a) facilitates the transfer of digital test vector data from CAE to ATE environments; (b) specifies pattern, format, and timing information sufficient to define the application of digital test vectors to a DUT; and (c) supports the volume of test vector data generated from structured tests.
Keywords: automatic test pattern generator (ATPG), built-in self-test (BIST), computer-aided engineering (CAE), cyclize, device under test (DUT), digital test vectors, event, functional vectors, pattern, scan vectors, signal, structural vectors, timed event, waveform, waveshape

IEEE Introduction

Standard Test Interface Language (STIL) was initially developed by an ad-hoc consortium of test equipment vendors, computer-aided engineering (CAE) and computer-aided design (CAD) vendors, and integrated circuit (IC) manufacturers, to address the lack of a common solution for transferring digital test data from the generation environment to the test equipment.

The need for a common interchange format for large volumes of digital test data was identified as an overriding priority for the work; as such, the scope of the work was constrained to those aspects of the test environment that contribute significantly to the volume issue, or are necessary to support the comprehension of that data. Binary representations of data were a key consideration in these efforts, resulting in a proposal to incorporate the compression of files as part of this standard.

Limiting the scope of any standards project is a difficult thing to do, especially for a room full of engineers. However, issues that did not impact the scope as identified were dropped from consideration in this version of the standard. Subclause 1.1 covers, specifically, the capabilities that are not intended to be part of this first standard.

Early work in this consortium consisted of identifying the requirements necessary to address this problem and reviewing existing options and languages in the industry. All options proposed fell short of addressing the requirements, and the consortium started to define a new language. This work was executed with heavy leverage from some existing languages and environments, and STIL owes much to the groundwork established by these other languages.

STANDARD TEST INTERFACE LANGUAGE (STIL) FOR DIGITAL TEST VECTOR DATA

1. Overview

Standard Test Interface Language (STIL) is a standard language that provides an interface between digital test generation tools and test equipment. STIL may be directly generated as an output language of a test generation tool, or it may be used as an intermediate format for subsequent processing. Figure 1 shows STIL usage in a "pipe" format. This is meant solely as a visual analogy to emphasize the high-volume/high-throughput requirements. It is not meant to represent physical structures or implementation requirements.

STIL is a representation of information needed to define digital test operations in manufacturing tests. STIL is not intended to define how the tester implements that information. While the purpose of STIL is to pass test data into the test environment, the overall STIL language is inherently more flexible than any particular tester. Constructs may be used in a STIL file that exceed the capability of a particular tester. In some circumstances, a translator for a particular type of test equipment may be capable of restructuring the data to support that capability on the tester; in other circumstances, separate tools may operate on that data to provide that restructuring. In all circumstances, it is desirable to provide the capability to check the data against the constraints of a tester. This capability is referred to as Tester Rules Checking and is the domain of tools that operate on STIL data. As such, Tester Rules Checking operations are outside the scope of this standard.

Figure 2 shows how STIL fits into the data flow between computer-aided engineering (CAE)/simulation and the test environment. In this figure, STIL is shown as both the input and output of "STIL Manipulation Tools." STIL represents patterns as a series of cyclized waveforms that are executed sequentially. The waveform representation can be as simple as a "print-on-change" set of events, or a complex set of parameterized events. Hence, tools may be required to manipulate the data according to the requirements of a particular class of device, simulation, or tester. The output of that manipulation is still represented in STIL.

Another issue presented in Figure 2 is the need for data from the tester to be transmitted back to the CAE/simulation environment for the purpose of correlating simulation data to tester data. Although this is recognized as an important aspect of testing digital devices, it does not represent the data volume that the patterns themselves do, and is not specifically supported in this version of the standard.

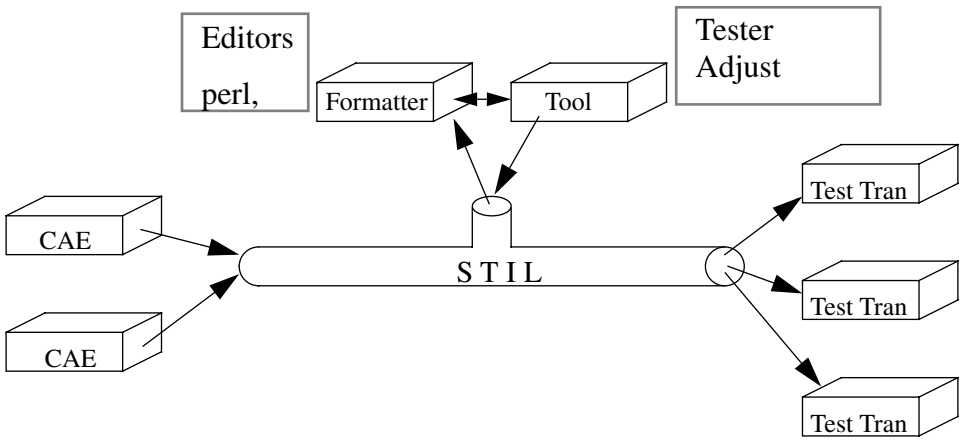

Figure 1—A conduit for transporting data from CAE to ATE

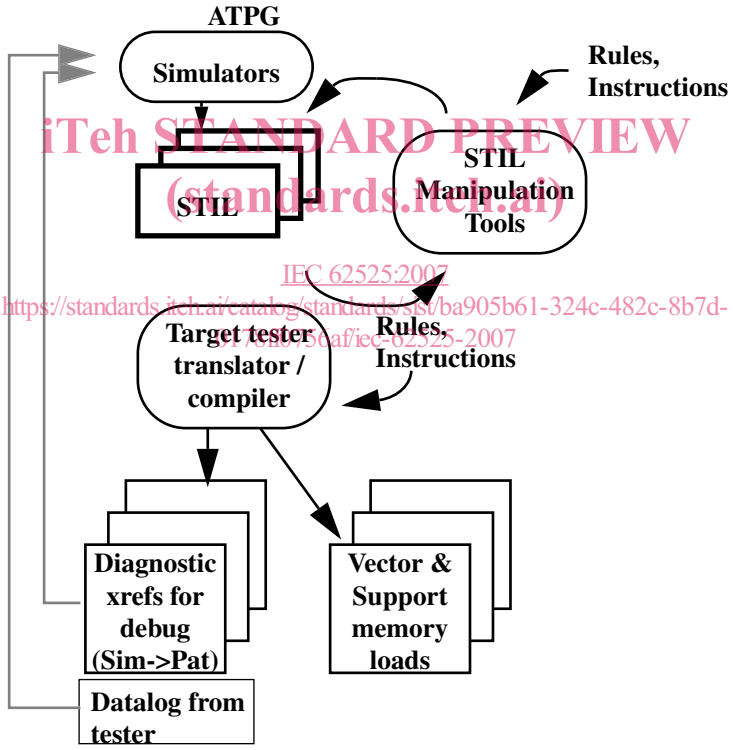

Figure 2—STIL usage model

1.1 Scope

This standard defines a test description language that:

a) Facilitates the transfer of large volumes of digital test vector data from CAE environments to automated test equipment (ATE) environments;

b) Specifies pattern, format, and timing information sufficient to define the application of digital test vectors to a device under test (DUT);

c) Supports the volume of test vector data generated from structured tests such as scan/automatic test pattern generation (ATPG), integral test techniques such as built-in self test (BIST), and functional test specifications for IC designs and their assemblies, in a format optimized for application in ATE environments.

In setting the scope for any standard, some issues are defined to not be pertinent to the initial project. The following is a partial list of issues that were dropped from the scope of this initial project:

— Levels: A key aspect of a digital test program is the ability to establish voltage and current parameters (levels) for signals under test. Level handling is not explicitly defined in the current standard, as this information is both compact (not presenting a transportation issue) and commonly established independently of digital test data, requiring different support mechanisms outside the current scope of this standard. Termination values may affect levels.

— Diagnostic/fault-tracing information: The goal of this standard is to optimally present data that needs to be moved onto ATE. While diagnostic data, fault identification data, and macro/design element correspondence data can fall into this category (and is often fairly large), this standard is also focused on integrated circuit and assemblies test, and most debug/failure analysis occurs separately from the ATE for these structures. Note that return of failure information (for off-ATE analysis) is also not part of the standard as currently defined.

— Datalogging mechanisms, formatting, and control usually are not defined as part of this current standard.

— Parametric tests are not defined as an integral part of this standard, except for optional pattern labels that identify potential locations for parametric tests, such as I_{DDQ} tests or alternating current (AC) timing tests.

— Program flow: Test sequencing and ordering are not defined as part of the current standard except as necessary to define collections of digital patterns meant to execute as a unit.

— Binning constructs are not part of the current standard.

— Analog or mixed-signal test: While this is an area of concern for many participants, at this point transfer of analog test data does not contribute to the same transportation issue seen with digital data.

— Algorithmic pattern constructs (such as sequences commonly used for memory test) are not currently defined as part of the standard.

— Parallel test/multisite test constructs are not an integral part of the current environment.

— User input and user control/options are not part of the current standard.

— Characterization tools, such as shmoo plots, are not defined as part of the current standard.

1.2 Purpose

This standard addresses a need in the integrated circuit (IC)[1] test industry to define a standard mechanism for transferring the large volumes of digital test data from the generation environment through to test. The environment today contains unique output formats of existing CAE tools, individual test environments of IC manufacturers, and proprietary IC ATE input interfaces. As each of these three arenas solves individual problems, together they have created a morass of interfaces, translators, and software environments that provide no opportunity to leverage common goals and result in much wasted efforts re-engineering solutions. As device density increases, the magnitude of test data threatens to shift the test bottleneck from the generation process to the processes necessary solely to maintain and transport this data. These two factors threaten to eliminate any productive work performed in this area unless a viable standard is defined.

With a common standard for CAE and IC ATE environments, the generation, movement, and processing of this test data is greatly facilitated. This standard also allows for immediate access to test equipment supporting this standard, which benefits both ATE and IC vendors reviewing this equipment.

This standard also serves as a catalyst for the development of a set of standard third party interface tools to both test and design aspects of IC device generation.

2. References

This standard shall be used in conjunction with the following standards. If the following publications are superseded by an approved revision, the revision shall apply.

IEEE Std 100-1996, The IEEE Standard Dictionary of Electrical and Electronics Terms, Sixth Edition.[2]

IEEE Std 260.1-1993, American National Standard Letter Symbols for Units of Measurement (SI Units, Customary Inch-Pound Units, and Certain Other Units).

ISO 2955:1983, Information processing—Representation of SI and other units in systems with limited character sets.[3]

ISO/IEC 9899:1999, Programming languages—C.[4]

3. Definitions, acronyms, and abbreviations

3.1 Definitions

For the purposes of this standard, the following terms and definitions apply. Additional terminology specific to this standard is found in Annex A. IEEE Std 100-1996, *The IEEE Standard Dictionary of Electrical and Electronics Terms, Sixth Edition*, should be referenced for terms not defined in this document.

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[1]The use of this term in this standard is meant only as a point of reference and not to indicate an explicit limitation or restriction of focus.

[2]IEEE publications are available from the Institute of Electrical and Electronics Engineers, 445 Hoes Lane, P.O. Box 1331, Piscataway, NJ 08855-1331, USA (http://www.standards.ieee.org/).

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