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IEEE 1450.1™

Standard for Extensions to Standard Test Interface Language (STIL) for Semiconductor Design Environments

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INTERNATIONAL ELECTROTECHNICAL COMMISSION

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STANDARD FOR EXTENSIONS TO STANDARD TEST INTERFACE LANGUAGE (STIL) FOR SEMICONDUCTOR DESIGN ENVIRONMENTS

FOREWORD

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IEEE Std	FDIS	Report on voting
1450.1(2005)	93/248/FDIS	93/259/RVD

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

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IEEE Standard for Extensions to Standard Test Interface Language (STIL) (IEEE Std 1450™-1999) for Semiconductor Design Environments

Sponsor

Test Technology Standards Committee
of the
IEEE Computer Society

Approved 9 June 2005

IEEE-SA Standards Board

Abstract: Standard Test Interface Language (STIL) provides an interface between digital test generation tools and test equipment. Extensions to the test interface language (contained in this standard) are defined that (1) facilitate the use of the language in the design environment and (2) facilitate the use of the language for large designs encompassing subdesigns with reusable patterns.

Keywords: advanced scan architecture, core, environment, fail feedback, lockstep, parallel patterns, parameterized data, pattern tiling, pragma, signal variable, system on chip (SoC), test protocol

IEEE Introduction

The Standard Test Interface Language (STIL) was initially developed by an ad hoc consortium of automatic test equipment vendors (ATE), electronic design automation vendors (EDA), and integrated circuit (IC) manufacturers to address the lack of a common solution for transferring digital test data from the generation environment to the test equipment.

The scope of the initial STIL standard was limited to satisfy the basic needs of pattern definition. Additional capabilities are developed as separate projects resulting in separate (dot) extensions to the initial STIL standard. The scope of this extension is defined in 1.1 and is primarily to address design needs.

Whereas the initial STIL standard was developed by reviewing many languages already in existence in the industry, this standard has been developed by inventing new capabilities in support of new device designs. The new language constructs have been added such that they do not alter in any way the initial definition of STIL, yet are syntactically compatible with the initial STIL language.

Much of the work to develop and validate these extensions has been done by prototyping on the part of the contributing companies.

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STANDARD FOR EXTENSIONS TO STANDARD TEST INTERFACE LANGUAGE (STIL) (IEEE Std 1450™-1999) FOR SEMICONDUCTOR DESIGN ENVIRONMENTS

1. Overview

STIL is an evolving standard being developed in support of various needs for interfacing between test generation tools and test equipment. IEEE Std 1450-1999 (STIL.0) [B3][1] forms the basis for this evolution. New "dot" standards (like this one) are being developed to address specific needs beyond STIL.0.

This (STIL.1) standard addresses design-related aspects of digital test data. This standard can also be viewed as the addition of advanced features to the STIL.0 baseline to allow for the usage of STIL in more complex applications, while leaving the basic standard unchanged as a vehicle for transmitting basic test data. The following is a brief overview of the new features in STIL.1 to support advanced applications such as (1) embedded cores,[2] (2) families of test patterns, (3) mapping to automated test equipment (ATE) systems,[3] (4) mapping to simulation, and (5) devices with advanced design for test (DFT). Please see Annex O for a list of specific statements for each of these features.

Environment mapping: Data for a device exist in many forms and in many other software environments. Examples include (1) simulation environment, (2) static analysis environment, (3) specific ATE system environment. The STIL Environment block is a new mechanism to relate STIL data to these other environments. No assumptions, expectations, or limitations are imposed on the other environments. It is just a way of relating one to the other.

Parameterized data: Much of STIL data are declarative in nature (i.e., it defines various static attributes of a device or pattern set). The addition of constant declarations, IntegerConstant and WFCConstant, allows a data set to be created that applies to a family of devices.

Complex test protocol definition: Test protocol definitions are usually contained in STIL procedures or MacroDefs and are used to specify the application of a series of data values to a device. STIL.0 supports scan chain data passing and simple WaveformCharacter (WFC) data passing via the # and % characters. STIL.1 enhances this capability by allowing the use of data substitution from SignalVariables and integer-

[1] The numbers in brackets correspond to those of the bibliography in Annex P.

[2] This standard contains syntax in support of embedded cores. See IEEE Std 1450.6™-2005 (Core Test Language) [B5] for the complete specification.

[3] This standard contains syntax in support of ATE systems. See IEEE P1450.3™ (Test Resource Constraints) [B4] for the complete specification.

Complex test protocol definition: Test protocol definitions are usually contained in STIL procedures or MacroDefs and are used to specify the application of a series of data values to a device. STIL.0 supports scan chain data passing and simple WaveformCharacter (WFC) data passing via the # and % characters. STIL.1 enhances this capability by allowing the use of data substitution from SignalVariables and integer-expressions. STIL.1 also enhances the functionality of Loops and Vectors and adds If/While decisions on pattern statements. These capabilities are needed for BIST, embedded cores, and various test access mechanisms.

Advanced scan architecture: Advanced DFT techniques require additional capabilities beyond what is defined in STIL.0, which includes multistate scan cells, reconfigurable scan-chains, and scan-chain indexing.

Run-time pattern decisions: The If, Else, While, and LoopData are new STIL.1 constructs that have been added for specification of pattern activity. These statements are needed in the specification of patterns to be run in the simulation environment. Although there is no standardization among ATE systems on run-time instructions for pattern execution, it is anticipated that restricted versions of these statements will be incorporated into ATE test patterns.

Pattern burst options: New variations on the PatternBurst have been added to allow for patterns running in parallel, patterns running in LockStep, and patterns that can be reordered. For parallel pattern execution, the specification for how the patterns fit together can be specified with the Fixed and Extend statements.

Enhanced user extensibility: The UserKeyword extensibility defined in STIL.0 has been extended to allow keywords to be defined on a per-block-type basis.

Signal relationships: Additional syntax is provided to allow the specification of relationships between signals. This process is preformed via \m to map WFCs to another WFC, \j to join WFCs, Extend to define behavior of signals beyond the bounds of a given pattern, and Fixed to restrict any further changes to signals within a pattern.

Fail feedback: Three new features are added to facilitate the processing of failure data from an ATE system back to design tools. The first is the X or cross-reference statement that allows the specification of where in a pattern/vector sequence a failure occurs. The second is the FailFeedback block for reporting fails. The third is the S/s timing event that allows for the specification of a data capture protocol for the purpose of capturing bulk fail data for processing.

1.1 Scope

Structures are defined in STIL to support usage as semiconductor simulation stimulus, including (1) mapping signal names to equivalent design references, (2) interface between scan and built-in self test (BIST) and the logic simulation, (3) data types to represent unresolved states in a pattern, (4) parallel or asynchronous pattern execution on different design blocks, and (5) expression-based conditional execution of pattern constructs.

Structures are defined in STIL to support the definition of test patterns for sub-blocks of a design[4] (i.e., embedded cores) such that these tests can be incorporated into a complete higher level device test.

Structures are defined in STIL to relate fail information from device testing environments back to original stimulus and design data elements.

[4]Syntax in this document that is used in the definition of patterns for sub-blocks is summarized in Annex O.

1.2 Purpose

The STIL language definition is enhanced to support the usage of STIL in the design environment, which includes extending the execution concept to support STIL as a stimulus language, to allow STIL to be used as an intermediate form of data, and to allow STIL to capture design information needed to port simulation data to device test environments.

In addition, define extensions to support the definition of subelement tests and to define the mechanisms to integrate those tests into a complete device test. This effort is to be performed in conjunction with IEEE Std 1500™-2005 [B6] and IEEE P1450.6 [B5], which are defining standards for the definition and integration of embedded cores.

Finally, define the constructs necessary to correlate test failure information back to the design environment, to allow debug and diagnosis operations to be performed based on failure information in STIL format.

2. Definitions, acronyms, and abbreviations

2.1 Definitions

For the purposes of this standard, the following terms and definitions apply. Additional terminology specific to this standard is found in Annex A. *The Authoritative Dictionary of IEEE Standards Terms* [B1] should be referenced for terms not defined in this clause.

2.1.1 automated test equipment (ATE): It refers to a tester that is capable of interfacing to a semiconductor device and executing test pattern data that is imported from a STIL file/stream.

2.1.2 built-in self-test (BIST): A design practice in which test logic is incorporated into the circuitry of a semiconductor device. This circuitry may provide completely autonomous testing of a device (i.e., without any requirement of a tester). It may be such that stimulation by an external tester is required; however, the STIL file may be substantially different from a device without this circuitry incorporated.

2.1.3 core: A component or module that contains separately developed functionality, integrated into a chip to provide additional overall functionality. *See also:* **System on Chip.**

2.1.4 electronic design automation (EDA): The set of software tools that are used for the design and creation of semiconductor chips. It includes the software tools that create the test patterns for the chips, which are often referred to as automated test pattern generators (ATPGs).

2.1.5 Standard Test Interface Language (STIL): The set of IEEE standards, including IEEE Std 1450-1999, and all dotted extensions, including this one.

2.1.6 System on Chip (SoC): An integrated circuit containing modules that are designed/integrated such that they can be tested independently and have associated test patterns for each module.

2.1.7 WaveformCharacter (WFC): A symbol used for referencing waveforms.

NOTE—See Annex A.[5]

[5]Notes in text, tables, and figures are given for information only, and do not contain requirements needed to implement the standard.

2.1.8 WaveformTable (WFT): An STIL block statement used to define waveforms across multiple signals and WFCs.

NOTE—See Annex A.

2.1.9 WaveformGenerationLanguage (WGL): A proprietary standard that was, in part, used as the basis for STIL.0.

2.2 Acronyms and abbreviations

ATE	automated test equipment
BIST	built-in self-test
DFT	design for test
DUT	device under test
EDA	electronic design automation
STIL	Standard Test Interface Language
STIL.0	IEEE Std 1450-1999 [B3]
STIL.1	this standard
WFC	WaveformCharacter
WFT	WaveformTable
WGL	WaveformGenerationLanguage

3. Structure of this standard

This standard is an adjunct to STIL.0. The conventions established and defined in STIL.0 are used in this standard and are included verbatim.

Many clauses in this standard add additional constructs to existing clauses in STIL.0 and are so identified in the title. The Environment block is a new construct introduced in this standard. All clauses in this standard are normative. Example code is provided within each clause. More complete examples are provided in the annexes, which are informative.

The following is a copy of the conventions as defined in STIL.0 and adhered to in this standard.

Different fonts are used as follows:

— SMALL CAP TEXT indicates user data.

— `Courier text` indicates code examples.

In the syntax definitions

a) SMALL CAP TEXT indicates user data.

b) **Bold text** indicates keywords.

c) *Italic text* references metatypes.

d) () indicates optional syntax that may be used zero or one time.

e) ()+ indicates syntax that may be used one or more times.

f) ()* indicates optional syntax that may be used zero or more times.

g) <> indicates multiple-choice arguments or syntax.

In the syntax explanations, the verb “shall” indicates mandatory requirements. The meaning of a mandatory requirement varies for different readers of the standard:

— To developers of tools that process STIL (readers), “shall” denotes a requirement that the standard imposes. The resulting implementation is required to enforce this requirement and issue an error if the requirement is not met by the input.

— To developers of STIL (writers), “shall” denotes mandatory characteristics of the language. The resulting output must conform to these characteristics.

— To the users of STIL, “shall” denotes mandatory characteristics of the language. Users may depend on these characteristics for interpretation of the STIL source.

The language definition clauses contain statements that use the phrase “it is an error” and “it may be ambiguous.” These phrases indicate improperly defined STIL information. The interpretation of these phrases will differ for the different readers of this standard in the same way that “shall” differs, as identified here in the dashed list.

4. STIL syntax description

This clause defines extensions to STIL.0, Clause 6.

All constructs and restrictions for STIL.0, Clause 6 are in effect here, with the following additions:

— Additional STIL reserved words are defined (see Table 1) for the top-level blocks specified within this standard.

— Additional STIL reserved characters are defined (see Table 2) for the new characters specified within this standard.

— Additional definition of signal and group naming, as well as name space resolution, is provided in this clause.

— Extensions to the expression environment are defined in this standard. Expression definitions (which are part of Clause 5 in STIL.0) are now specified in a separate clause (Clause 6 in this standard).

4.1 Reserved words

Table 1 lists all STIL reserved words defined by this standard. Only top-level block names that are defined in this standard are added to the STIL reserved word list. New keywords that appear inside of top-level blocks are not restricted from usage in other contexts outside of the definition of that keyword. No change to reserved words as defined in STIL.0 is made by this standard.

Table 1—Additions to STIL reserved words

Environment
PatternFailReport, Pragma
Variables