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IEEE 1500™

Standard Testability Method for Embedded Core-based Integrated Circuits

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STANDARD TESTABILITY METHOD
FOR EMBEDDED CORE-BASED INTEGRATED CIRCUITS

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1500(2005)	93/250/FDIS	93/261/RVD

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IEEE-SA Standards Board

Abstract: This standard defines a mechanism for the test of core designs within a system on chip (SoC). This mechanism constitutes a hardware architecture and leverages the core test language (CTL) to facilitate communication between core designers and core integrators.
Keywords: core test, embedded core test, IP test, test reuse

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IEEE Introduction

IEEE Std 1500 is a scalable standard architecture for enabling test reuse and integration for embedded cores and associated circuitry. It foregoes addressing analog circuits and focuses on facilitating efficient test of digital aspects of systems on chip (SoCs). IEEE Std 1500 has serial and parallel test access mechanisms (TAMs) and a rich set of instructions suitable for testing cores, SoC interconnect, and circuitry. In addition, IEEE Std 1500 defines features that enable core isolation and protection. IEEE Std 1500 will reduce test cost through improved automation, promote good design-for-test (DFT) technique, and improve test quality through improved access.

Core test language (CTL) is the official mechanism for describing IEEE 1500 wrappers and test data associated with cores. CTL is defined in IEEE P1450.6 ™[a] and was originally begun as part of the development of IEEE Std 1500.

IEEE Std 1500 was broadly influenced by the past work of the IEEE Std 1149.1™ Working Group and has several members from that group. IEEE Std 1149.1 and IEEE Std 1500 have similar goals at different levels of integration. IEEE Std 1149.1 describes a wrapper architecture and access mechanism designed for the purpose of testing components of a board whereas IEEE Std 1500 has a similar structure targeted towards testing cores in an SoC.

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IEEE Std 1500 has been a continuous effort for its participants due to the goal of resolving the needs of reconciling and accommodating disparate test strategies and motives. The greatest effort has been put into supporting as many requirements as possible while still producing a cohesive and consistent standard.

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Objective of the IEEE 1500 effort

The Embedded Core Test Working Group was approved in 1997 with the charter to develop a standard test method for integrated circuits (ICs) containing embedded cores, i.e., reusable megacells. That method would be independent of the underlying functionality of the IC or its individual embedded cores. The method will create the necessary testability requirements for detection and diagnosis of such ICs, while allowing for ease of interoperability of cores originated from distinct sources. This method will be usable for all classes of digital cores including hierarchical ones (subclause 15.1 discusses hierarchical core-wrapper configurations).

In order to satisfy that charter, the Embedded Core Test Working Group was organized into several task forces:

Core Test Language

Scalable Architecture

Compliance Definition/Information Model

Terminology/Glossary

Edition

Mergeable Cores Test

Benchmarking

Industry & Media Relations

[a]Information on references can be found in Clause 2.

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Achievements

Since its inception, the Embedded Core Test Working Group has produced eight drafts of the preliminary standard, considering all aspects of core-based test. Due concern has been given to ensuring that a broad spectrum of users will be satisfied through flexibility. Both serial and parallel TAMs were developed. A definition for core wrappers was created, and a set of instructions developed. The CTL was begun, and an information model and compliance definition using that language were developed.

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STANDARD TESTABILITY METHOD FOR EMBEDDED CORE-BASED INTEGRATED CIRCUITS

1. Overview

IEEE Std 1500™ defines a scalable architecture for independent, modular test development and test application for embedded design blocks and also enables test of the external logic surrounding these cores. Modular testing is typically a requirement for embedded nonlogic blocks, such as memories, and for embedded predesigned nonmergeable intellectual property (IP) cores. In addition, the IEEE 1500 architecture can also be used to partition large design blocks into smaller blocks of more manageable size and to facilitate test reuse for blocks that are reused from one system-on-chip (SoC) design to the next.

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The IEEE 1500 architecture comprises hardware requirements, through the definition of a standardized core wrapper, and uses a test-specific language to communicate information between core providers and core users. This language is the IEEE P1450.6™ [1] core test language (CTL). Although IEEE Std 1500 limited itself to test aspects internal to nonmergeable cores, careful consideration was given to the interoperability of such cores, resulting in plug-and-play (PnP) requirement definitions. SoC-specific issues such as those related to the design of test access mechanisms (TAMs) are excluded from this standard and assumed to be addressed by the SoC designer.

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IEEE Std 1500 specifically focuses on defining test requirements for unidirectional non-tristate digital terminals, as these represent a minimum and mandatory set of requirements upon which the more complex bidirectional terminals are based. It is, therefore, implied that support for bidirectional or tristatable terminals is provided only to the extent that the individual unidirectional terminals, i.e., the bidirectional or tristatable terminal, are available for IEEE 1500 wrapper insertion. In addition, the hardware architecture defined in this standard anticipates a synchronous wrapper design methodology.

While IEEE Std 1500 does not discuss chip-level design, the architecture defined in this standard does not prevent interfacing with IEEE 1149.1™-based standards. An example of this interface is provided in Annex C for the reader's benefit.

All rules described in this standard apply to the case where the IEEE 1500 wrapper is enabled (the wrapper logic actively participates in the test of the core) except rules specific to the Wrapper Disabled state of the IEEE 1500 wrapper. In Wrapper Disabled state, the IEEE 1500 wrapper is disabled, allowing functional

[1]Information on references can be found in Clause 2.

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operation of the wrapped core. IEEE P1450.6 constructs were added to this standard, where appropriate, to further guide the reader. It is anticipated that the reader will refer to these CTL constructs documented in IEEE P1450.6. Additional discussion that complements the body of this standard are presented in annex clauses:

— Annex A contains the legend for IEEE 1500 wrapper cells.

— Annex B shows examples of IEEE 1500 wrapper cells.

— Annex C presents similarities between IEEE Std 1500 and IEEE Std 1149.1 and discusses an example interface between IEEE Std 1500 and IEEE Std 1149.1.

1.1 Scope

IEEE Std 1500 has developed a standard design-for-testability method for integrated circuits (ICs) containing embedded nonmergeable cores. This method is independent of the underlying functionality of the IC or its individual embedded cores. The method creates the necessary requirements for the test of such ICs, while allowing for ease of interoperability of cores that may have originated from different sources.

1.2 Purpose

The aim of IEEE Std 1500 is to provide a consistent scalable solution to the test reuse challenges specific to the reuse of nonmergeable cores, while preserving the IP aspects that are often associated with these cores. This objective is achieved through provision of a core-centric methodology that enables successful integration of cores into SoCs.

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IEEE Std 1500 provides a bridge between core providers and core users and also facilitates the automation of test data transfer and reuse between these two entities via the use of the IEEE P1450.6 CTL. This automation relies on information requirements (the information model) placed on the core provider to ensure that the core can be successfully integrated by the core user. The result is shorter time to market for core providers and core users.

The data transfer and reuse from the core provider to the core user are based on the premise that the core test data are left unchanged, while the test protocol is adapted from the IEEE 1500 hardware interface to the SoC.

2. Normative references

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments or corrigenda) applies.

IEEE Std 1149.1, IEEE Standard Test Access Port and Boundary-Scan Architecture.[2]

IEEE P1450.6, Draft Standard for Standard Test Interface Language (STIL) for Digital Test Vector Data—Core Test Language (CTL), http://grouper.ieee.org/groups/ctl/.

[2]IEEE publications are available from the Institute of Electrical and Electronics Engineers, 445 Hoes Lane, Piscataway, NJ 08854, USA (http://standards.ieee.org/).

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3. Definitions, acronyms, and abbreviations

This clause lists some definitions of terms that have been used throughout this standard. In addition, a list of acronyms and abbreviations is also provided. The criteria for differentiating various terms are based on the following rules:

a) General terminology in the scope of electrical engineering and/or test technology, which do not influence the definition of this standard itself.
   1) These terms are used in this standard without further explanation. It is assumed that the readership has sufficient background knowledge to understand these terms.
   2) Some of these terms may already be defined in *The Authoritative Dictionary of IEEE Standards Terms*. Therefore, someone looking for a particular definition could always consult *The Authoritative Dictionary* to verify the meaning of the term.

b) Terms that are specific to this standard
   1) These terms are defined in this clause.
   2) General definitions are valid throughout this standard.
   3) Local definitions are relevant only to a specific clause of this standard.

Effort has been made to achieve consistent usage of all terms (e.g., wrapper, TAM).

3.1 Definitions

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3.1.1 access mechanisms: Mechanisms by which signals may be propagated to and from a core, from either embedded circuitry or from the primary inputs and outputs of the system chip. There are two types of access mechanisms:

(a) Functional access: The mechanism for moving stimuli to and observing responses from a core or user-defined logic (UDL) during functional operation or normal mode.

b) Test access: The mechanism for moving stimuli to and observing responses from a core or UDL during nonfunctional operation or test mode.

3.1.2 auxiliary clock (AUXCK): A functional clock that may be used in conjunction with wrapper clock (WRCK) during core test for capturing, shifting, updating, and optionally transferring test data in a wrapper.

3.1.3 bypass: As applied to core wrappers, an abbreviated sequential path connecting a wrapper serial input (WSI) to a wrapper serial output (WSO).

3.1.4 captureWR: A wrapper terminal used to enable and control a Capture operation in the selected IEEE 1500 wrapper register (WR).

3.1.5 cell functional input (CFI): For input wrapper cells, the cell's input, which is connected to a wrapper functional input (WFI); for output wrapper cells, the cell's input, which is connected to a core output.

NOTE—See CFI pin in Figure 16.

3.1.6 cell functional output (CFO): For input wrapper cells, the cell's output, which is connected to a core input; for output wrapper cells, the cell's output, which is connected to a wrapper functional output (WFO).

NOTE—See CFO pin in Figure 16.

3.1.7 cell test input (CTI): A wrapper boundary register (WBR) cell's test data input.

3.1.8 cell test output (CTO): A wrapper boundary register (WBR) cell's test data output.

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3.1.9 control: The process of applying test pattern stimuli.

3.1.10 core: Predesigned circuit block that can be tested as an individual unit.

3.1.11 core data register (CDR): Optional data register that belongs to a core being wrapped.

3.1.12 core input: An input terminal of an unwrapped core.

3.1.13 core integrator: An entity that incorporates one or more cores into an system on chip (SoC).

3.1.14 core isolation: A test mode feature preventing core-to-core or core-to-UDL (i.e., user-defined logic) interaction.

3.1.15 core output: An output terminal of an unwrapped core.

3.1.16 core provider: An entity that designs cores that can be reused in other designs.

3.1.17 core test: A test methodology that is applied to an embedded core.

3.1.18 core test language (CTL): A standard language for core suppliers to provide test data that can be used to test a core once it is integrated into a system on chip (SoC). The language presents a format to describe test and support data so that the core can be effectively integrated, reused and tested.

NOTE—See IEEE P1450.6 reference documentation.

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3.1.19 dedicated shift path: A shift path comprising storage elements that do not participate in functional operation.

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3.1.20 dedicated wrapper (cell): A wrapper style that does not share hardware with core functionality. This style allows certain test operations to occur concurrently and transparently during functional operation. This definition could apply to individual cells.

3.1.21 external safe state: A configuration of safe state in which the outputs of a core are in a state that prevents them from interfering with a block of logic outside the core. *See also* **internal safe state**; **safe state**.

3.1.22 firm core: A predesigned block of functional logic such as a macro, megacell, or memory that has a process technology-dependent netlist representation and may be amenable to some modification.

3.1.23 hard core: A predesigned block of functional logic such as a macro, megacell, or memory that has a physical implementation that cannot be modified.

3.1.24 hybrid instruction: A wrapper instruction that has mixed use of wrapper serial port (WSP) and wrapper parallel port (WPP) terminals.

3.1.25 input cell: A wrapper boundary register (WBR) cell that is provided on a core input.

3.1.26 internal safe state: A configuration of safe state whereby a core is protected from the impact of a test outside the core. *See also* **external safe state**; **safe state**.

3.1.27 interoperability: *See* **plug-and-play (PnP)**.

3.1.28 inward facing (IF) mode: The test mode where core inputs are controlled by the wrapper boundary register (WBR) and core outputs are observed by the WBR.

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3.1.29 mergeable core: With respect to testability, a core that can be integrated with other cores and user-defined logic (UDL) into a system on chip (SoC) so that a uniform design-for-test (DFT) methodology can be applied across the entire system. A typical mergeable core is provided using a register transfer level (RTL) or gate-level description.

3.1.30 merged core: With respect to testability, a core that is integrated with other cores and user-defined logic (UDL) into a system on chip (SoC) so that a uniform design-for-test (DFT) methodology could be applied across the entire system.

3.1.31 nonmergeable core: With respect to testability, a core that cannot be integrated to apply a uniform design-for-test (DFT) methodology to the entire system on chip (SoC). A typical nonmergeable core comes with a physical design implementation that does not accommodate modification of the test methodology. A nonmegeable core may be represented as a block-box design, making standard automatic test pattern generation (ATPG) impossible on such a core.

3.1.32 nonmerged core: With respect to testability, a core that has not been integrated with other cores and user-defined logic (UDL) into a system on chip (SoC) so that a uniform design-for-test (DFT) methodology could be applied across the entire system.

3.1.33 normal mode: The mode in which the wrapper boundary register (WBR) does not interfere with the functional operation of a wrapped core.

3.1.34 observation: The process of monitoring pattern response.

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3.1.35 output cell: A wrapper boundary register (WBR) cell that is provided for a core output.

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3.1.36 outward facing (OF) mode: The test mode where wrapper functional outputs (WFOs) are controlled by the wrapper boundary register (WBR) and wrapper functional inputs (WFIs) are observed by the WBR.

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3.1.37 parallel instruction: A wrapper instruction that uses wrapper parallel port (WPP) terminals and also configures the wrapper bypass register (WBR) between wrapper serial input (WSI) and wrapper serial output (WSO).

3.1.38 pattern set: A collection of test vectors intended for manufacturing test. In the context of core test language (CTL), a pattern set is a collection of pattern constructs and their associated macros and procedures brought together with PatternBurst and PatternExecs.

3.1.39 plug-and-play (PnP): A minimum level of interoperability between various core wrappers in a system on chip (SoC).

3.1.40 safe data: Data that satisfy safe state configuration requirements. These data are user-defined.

3.1.41 safe state: A property whereby a test of one block of logic is prevented from interfering with or damaging another block of logic. *See also* **external safe state**; **internal safe state**.

3.1.42 selectWIR: The IEEE 1500 wrapper terminal that determines the selection of a wrapper register (WR). A value of 1 represents selection of the wrapper instruction register (WIR), and a value of 0 represents selection of a wrapper data register (WDR).

3.1.43 serial instruction: A wrapper instruction that exclusively uses wrapper serial port (WSP) terminals.

3.1.44 serial scan chain: The scan chain configuration inside a wrapped core where an internal scan chain is concatenated with the wrapper boundary register (WBR) chain for the purpose of running the WS_INTEST_SCAN instruction.

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