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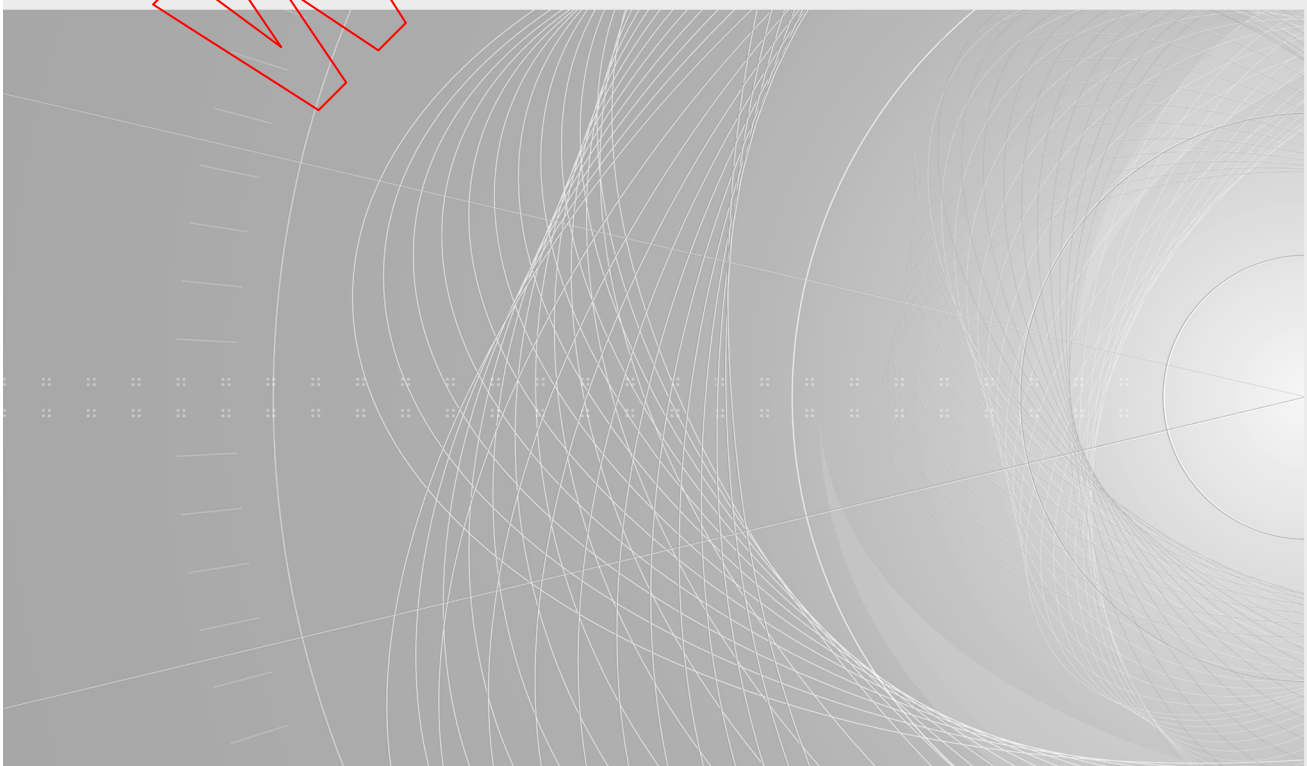
INTERNATIONAL STANDARD

IEEE 1800™

Standard for SystemVerilog – Unified Hardware Design, Specification, and Verification Language



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Standard For SystemVerilog – Unified hardware design, specification, and verification language

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IEEE Std	FDIS	Report on voting
1800(2005)	93/252/FDIS	93/263/RVD

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Sponsor

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and the

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Abstract: This standard provides a set of extensions to the IEEE 1364™ Verilog® hardware description language (HDL) to aid in the creation and verification of abstract architectural level models. It also includes design specification methods, embedded assertions language, testbench language including coverage and an assertions application programming interface (API), and a direct programming interface (DPI). This standard enables a productivity boost in design and validation and covers design, simulation, validation, and formal assertion-based verification flows.
Keywords: assertions, design automation, design verification, hardware description language, HDL, PLI, programming language interface, SystemVerilog, Verilog, Verilog programming interface, VPI