



SLOVENSKI STANDARD
SIST EN 61340-3-2:2007

01-december-2007

Nadomešča:
SIST EN 61340-3-2:2002

Elektrostatika - 3-2. del: Metode za simulacijo elektrostatičnih učinkov - Model stroja (MM) - Preskušanje sestavnih delov (IEC 61340-3-2:2006)

Electrostatics -- Part 3-2: Methods for simulation of electrostatic effects - Machine model (MM) electrostatic discharge test waveforms

Elektrostatik - Teil 3-2: Verfahren zur Simulation elektrostatischer Effekte - Prüfpulsformen der elektrostatischen Entladung für das Machine Model (MM)

Électrostatique -- Partie 3-2: Méthodes pour la simulation des effets électrostatiques - Formes d'onde d'essai des décharges électrostatiques pour les modèles de machine (MM)

Ta slovenski standard je istoveten z: EN 61340-3-2:2007

ICS:

17.220.99	Drugi standardi v zvezi z električno in magnetizmom	Other standards related to electricity and magnetism
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EUROPEAN STANDARD
NORME EUROPÉENNE
EUROPÄISCHE NORM

EN 61340-3-2

March 2007

ICS 17.220.99; 29.020

Supersedes EN 61340-3-2:2002

English version

**Electrostatics -
Part 3-2: Methods for simulation of electrostatic effects -
Machine model (MM) electrostatic discharge test waveforms
(IEC 61340-3-2:2006)**

Électrostatique -
Partie 3-2: Méthodes pour la simulation
des effets électrostatiques -
Formes d'onde d'essai des décharges
électrostatiques pour les modèles
de machine (MM)
(CEI 61340-3-2:2006)

Elektrostatik -
Teil 3-2: Verfahren zur Simulation
elektrostatischer Effekte -
Prüfwellenformen der elektrostatischen
Entladung für das Machine Model (MM)
(IEC 61340-3-2:2006)

ITeH STANDARD PREVIEW
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This European Standard was approved by CENELEC on 2007-02-01. CENELEC members are bound to comply with the CEN/CENELEC Internal Regulations which stipulate the conditions for giving this European Standard the status of a national standard without any alteration.

Up-to-date lists and bibliographical references concerning such national standards may be obtained on application to the Central Secretariat or to any CENELEC member.

This European Standard exists in three official versions (English, French, German). A version in any other language made by translation under the responsibility of a CENELEC member into its own language and notified to the Central Secretariat has the same status as the official versions.

CENELEC members are the national electrotechnical committees of Austria, Belgium, Bulgaria, Cyprus, the Czech Republic, Denmark, Estonia, Finland, France, Germany, Greece, Hungary, Iceland, Ireland, Italy, Latvia, Lithuania, Luxembourg, Malta, the Netherlands, Norway, Poland, Portugal, Romania, Slovakia, Slovenia, Spain, Sweden, Switzerland and the United Kingdom.

CENELEC

European Committee for Electrotechnical Standardization
Comité Européen de Normalisation Electrotechnique
Europäisches Komitee für Elektrotechnische Normung

Central Secretariat: rue de Stassart 35, B - 1050 Brussels

Foreword

The text of document 101/237/FDIS, future edition 2 of IEC 61340-3-2, prepared by IEC TC 101, Electrostatics, was submitted to the IEC-CENELEC parallel vote and was approved by CENELEC as EN 61340-3-2 on 2007-02-01.

This European Standard supersedes EN 61340-3-2:2002.

The major change of EN 61340-3-2:2007 is that it no longer contains the application to semiconductor devices.

It recognizes the direction of the IEC SMB (Standardization Management Board) in terms of considering inputs from TC 47 documents with regard to ESD test methods. TC 101 has revised this IEC 61340-3-2, concerning the machine model, in collaboration with the JWG of TC 47/TC 101. IEC 61340-3-2 incorporates TC 47 input, based on the corresponding TC 47 IEC 60749-27.

The following dates were fixed:

- latest date by which the EN has to be implemented at national level by publication of an identical national standard or by endorsement (dop) 2007-11-01
- latest date by which the national standards conflicting with the EN have to be withdrawn (dow) 2010-02-01

iTeh STANDARD PREVIEW (standard not final)

The text of the International Standard IEC 61340-3-2:2006 was approved by CENELEC as a European Standard without any modification. [SIST EN 61340-3-2:2007](https://standards.iteh.ai/catalog/standards/sist/aaa064b-2528-473c-878c-61340-3-2-2007)

In the official version, for Bibliography, the following note has to be added for the standard indicated:

IEC 60749-27 NOTE Harmonized as EN 60749-27:2006 (not modified).

NORME
INTERNATIONALE
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STANDARD

CEI
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61340-3-2

Deuxième édition
Second edition
2006-12

Électrostatique –

Partie 3-2:

Méthodes pour la simulation
des effets électrostatiques –

Formes d'onde d'essai des décharges
électrostatiques pour les modèles de
machine (MM)

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Electrostatics –

Part 3-2:

Methods for simulation of electrostatic effects –
Machine model (MM) electrostatic discharge
test waveforms

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International Electrotechnical Commission, 3, rue de Varembe, PO Box 131, CH-1211 Geneva 20, Switzerland
Telephone: +41 22 919 02 11 Telefax: +41 22 919 03 00 E-mail: inmail@iec.ch Web: www.iec.ch



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INTERNATIONAL ELECTROTECHNICAL COMMISSION

ELECTROSTATICS –

**Part 3-2: Methods for simulation of electrostatic effects –
Machine model (MM) electrostatic discharge test waveforms**

FOREWORD

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International Standard IEC 61340-3-2 has been prepared by IEC technical committee 101: Electrostatics.

This second edition cancels and replaces the first edition, published in 2002, and constitutes a technical revision.

The major change of this document is that it no longer contains the application to semiconductor devices.

It recognizes the direction of the IEC SMB (Standardization Management Board) in terms of considering inputs from TC 47 documents with regard to ESD test methods. TC 101 has revised this IEC 61340-3-2, concerning the machine model, in collaboration with the JWG of TC 47/TC 101. IEC 61340-3-2 incorporates TC 47 input, based on the corresponding TC 47 IEC 60749-27.

The text of this standard is based on the following documents:

FDIS	Report on voting
101/237/FDIS	101/239/RVD

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

The list of all parts of the IEC 61340 series, under the general title *Electrostatics*, can be found on the IEC website.

The committee has decided that the contents of this publication will remain unchanged until the maintenance result date indicated on the IEC web site under "<http://webstore.iec.ch>" in the data related to the specific publication. At this date, the publication will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

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ELECTROSTATICS –

Part 3-2: Methods for simulation of electrostatic effects – Machine model (MM) electrostatic discharge test waveforms

1 Scope

This part of IEC 61340 describes the discharge current waveforms used to simulate machine model (MM) electrostatic discharges (ESD) and the basic requirements for equipment used to develop and verify these waveforms.

This standard covers MM ESD waveforms for use in general test methods and for application to materials or objects, electronic components and other items for ESD withstand test or performance evaluation purposes. The specific application of these MM ESD waveforms to non-powered semiconductor devices is covered in IEC 60749-27.

2 Terms and definitions

For the purposes of this document, the following terms and definitions apply.

2.1 unit under test UUT

material, object, item or product to be subjected to the MM ESD test

2.2 UUT failure

condition in which a UUT does not meet one or more specified parameters as a result of the ESD test

2.3 ESD withstand voltage

maximum applied ESD voltage level that does not cause failure parameter limits to be exceeded provided that all UUTs stressed at lower levels have also passed

3 Equipment

3.1 MM ESD waveform generator

This equipment produces an electrostatic discharge current pulse simulating a MM ESD event for application to the UUT. The equivalent waveform generator circuit and tester evaluation loads are illustrated in Figure 1.

3.2 Waveform verification equipment

Equipment capable of verifying the MM current waveform is defined in this standard. This equipment includes, but is not limited to, a waveform recording system, a high-voltage resistor and a current transducer.

3.2.1 Waveform recording system

The waveform recording system shall have a minimum single shot bandwidth of 350 MHz.

3.2.2 Evaluation loads

Two evaluation loads are necessary to verify the functionality of the waveform generator:

- a) load 1: a shorting wire;
- b) load 2: a 500 Ω low-inductance resistor with a tolerance of ± 1 % appropriately rated for the voltages that will be used for waveform qualification.

The lead length of the evaluation loads (shorting wire or resistor) shall be as short as possible consistent with connecting the evaluation load to the appropriate reference terminals (A and B in Figure 1) while passing through the current transducer.

3.2.3 Current transducer

The current transducer shall have a minimum bandwidth of 350 MHz.

4 MM current waveform requirements

4.1 General

Prior to UUT testing, the MM ESD waveform generator qualification shall ensure the waveform integrity of the discharge current through both a shorting wire and a resistive load. The shorting wire waveform requirements are specified in Figure 2 for all positive and negative voltages defined in Table 1, while the resistive load waveform requirements for ± 400 V are shown in Figure 3 and Table 1.

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4.2 Waveform qualification and verification

Equipment qualification shall be performed during initial acceptance testing. Re-qualification is required whenever equipment repairs are made that may affect the waveform. Additionally, the waveforms shall be verified periodically. If a test fixture or circuit-board is used to perform UUT testing, the test fixture (board) shall also be used during equipment qualification tests. In case the waveform no longer meets the waveform parameters described in Table 1 and Figures 2 and 3, all ESD testing performed after the previous satisfactory waveform check shall be considered invalid.