# IEC 62386-210

Edition 1.0 2011-04

# INTERNATIONAL STANDARD

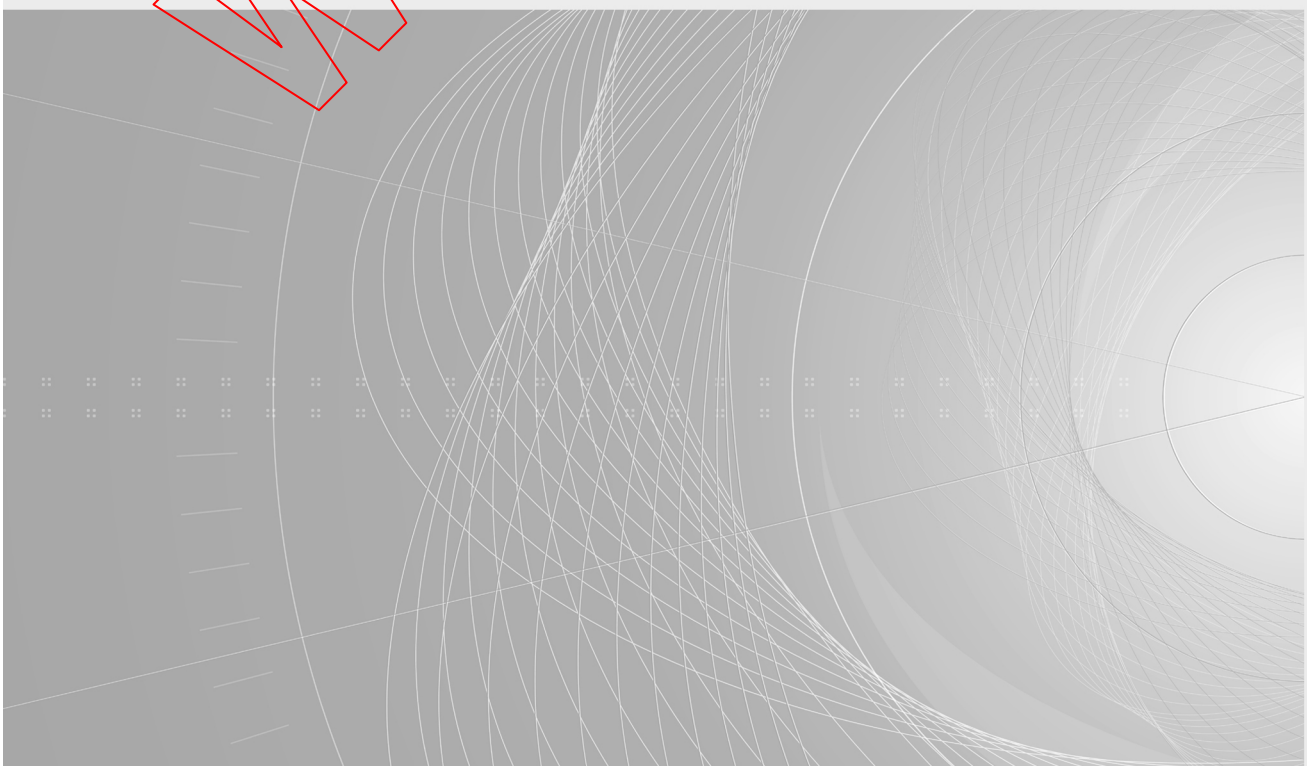
# NORME INTERNATIONALE



**Digital addressable lighting interface –**
**Part 210: Particular requirements for control gear – Sequencer (device type 9)**

**Interface d'éclairage adressable numérique –**
**Partie 210: Exigences particulières pour les appareillages de commande – Séquenceur (dispositifs de type 9)**





IEC 62386-210:2011

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## Digital addressable lighting interface – Part 210: Particular requirements for control gear – Sequencer (device type 9)

## Interface d'éclairage adressable numérique – Partie 210: Exigences particulières pour les appareillages de commande – Séquenceur (dispositifs de type 9)



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INTERNATIONAL ELECTROTECHNICAL COMMISSION

# DIGITAL ADDRESSABLE LIGHTING INTERFACE –

# Part 210: Particular requirements for control gear – Sequencer (device type 9)

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International Standard IEC 62386-210 has been prepared by subcommittee 34C: Auxiliaries for lamps, of IEC technical committee 34: Lamps and related equipment.

The text of this standard is based on the following documents:

| CDV | Report on voting |
|---|---|
| 34C/915/CDV | 34C/938/RVC |

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

This Part 210 is intended to be used in conjunction with IEC 62386-101 and IEC 62386-102, which contain general requirements for the relevant product type (control gear or control devices).

A list of all parts of the IEC 62386 series, under the general title *Digital addressable lighting interface* can be found on the IEC website.

The committee has decided that the contents of this publication will remain unchanged until the stability date indicated on the IEC web site under "http://webstore.iec.ch" in the data related to the specific publication. At this date, the publication will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

# INTRODUCTION

This first edition of IEC 62386-210 is published in conjunction with IEC 62386-101 and IEC 62386-102. The division of IEC 62386 into separately published parts provides for ease of future amendments and revisions. Additional requirements will be added as and when a need for them is recognised.

This International Standard, and the other parts that make up the IEC 62386-200 series, in referring to any of the clauses of IEC 62386-101 or IEC 62386-102, specifies the extent to which such a clause is applicable and the order in which the tests are to be performed. The parts also include additional requirements, as necessary. All parts that make up the IEC 62386-200 series are self-contained and therefore do not include references to each other.

Where the requirements of any of the clauses of IEC 62386-101 or IEC 62386-102 are referred to in this International Standard by the sentence "The requirements of IEC 62386-1XX, clause ‘n’ apply", this sentence is to be interpreted as meaning that all requirements of the clause in question of Part 101 or Part 102 apply, except any which are inapplicable to the specific type of lamp control gear covered by Part 210.

All numbers used in this International Standard are decimal numbers unless otherwise noted. Hexadecimal numbers are given in the format 0xVV, where VV is the value. Binary numbers are given in the format XXXXXXXXb or in the format XXXX XXXX, where X is 0 or 1; 'x' in binary numbers means 'don't care'.

# DIGITAL ADDRESSABLE LIGHTING INTERFACE –

# Part 210: Particular requirements for control gear – Sequencer (device type 9)

## 1 Scope

This International Standard specifies a protocol and test procedures for the control by digital signals of electronic control gear working as automatic sequencers.

## 2 Normative references

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 62386-101:2009, *Digital addressable lighting interface – Part 101: General requirements – System*

IEC 62386-102:2009, *Digital addressable lighting interface – Part 102: General requirements – Control gear*



## 3 Terms and definitions

For the purposes of this document, the terms and definitions given in Clause 3 of IEC 62386-101:2009 and Clause 3 of IEC 62386-102:2009 apply, with the following additional definitions.

**3.1**
**multi channel device**
device which provides more than one output for controlling light sources

NOTE The individual outputs can have different states at the same time.

**3.2**
**point**
tuple consisting of a sequencer fade time, a hold time and an arc power level for each output channel

NOTE A point is reached when the sequencer fade time of this point has expired.

**3.3**
**next point**
point following the current point in a sequence

**3.4**
**previous point**
point preceding the current point in a sequence

**3.5**
**pointer**
contents of a register used as reference to the starting point of a sequence

NOTE For this purpose, a register may be one of the scenes 0 to 15 or the POWER ON LEVEL or the SYSTEM FAILURE LEVEL.

## 4 General description

The requirements of Clause 4 of IEC 62386-101:2009 and Clause 4 of IEC 62386-102:2009 shall apply.

## 5 Electrical specifications

The requirements of Clause 5 of IEC 62386-101:2009 and Clause 5 of IEC 62386-102:2009 shall apply.

## 6 Interface power supply

The requirements of Clause 6 of IEC 62386-101:2009 and Clause 6 of IEC 62386-102:2009 shall apply, if a power supply is integrated with the gear.

## 7 Transmission protocol structure

The requirements of Clause 7 of IEC 62386-101:2009 and Clause 7 of IEC 62386-102:2009 shall apply.



## 8 Timing

The requirements of Clause 8 of IEC 62386-101:2009 and Clause 8 of IEC 62386-102:2009 shall apply.



## 9 Method of operation

The requirements of Clause 9 of IEC 62386-101:2009 and Clause 9 of IEC 62386-102:2009 shall apply with the following exceptions:

*Amendments to Clause 9 of IEC 62386-102:2009:*

*Replacement:*

### 9.2 Power-on

Control gear shall start to react properly to commands not later than 0,5 s after power-on. If no command affecting power level is received before 0,6 s after mains power-on, the gear shall proceed as follows:

If the pointer control register CONTROL 253 contains 0, the control gear shall go to POWER ON LEVEL immediately without fading, unless 'MASK' is stored as the POWER ON LEVEL, in which case the control gear shall go to the most recent arc power level or start the most recent sequence at its starting point.

If the pointer control register CONTROL 253 contains a value other than 0, then the contents of the POWER ON LEVEL shall be used as pointer to the starting point of a sequence. If the Pointer Control Register CONTROL 253 contains 'MASK', the control gear shall run through the sequence until stopped by command. Otherwise, the number of times the gear runs through the sequence shall be given by the contents of CONTROL 253.

Clearly, there shall be an interval of at least 0,1 s during which it shall be possible for a control device to send an arc power control command which shall be obeyed immediately, thereby preventing the gear from processing the POWER-ON LEVEL as described.

NOTE 1 Different manufacturers' control gear may react in different ways to relative arc power commands (such as STEP DOWN) during the 0,1 s period mentioned above.

NOTE 2 Some control gear may have a preheating or ignition phase (see 9.7 of IEC 62386-102:2009).

NOTE 3 Different manufacturers' control gear may restore either the most recent actual arc power level or the most recent target arc power level if 'MASK' is stored as POWER-ON LEVEL.

### 9.3 Interface-failure

If the interface idle voltage remains below the specified receiver high level range (see IEC 62386-101:2009, Clause 5) for more than 500 ms, the control gear shall proceed as follows:

If the pointer control register CONTROL 254 contains 0, the control gear shall go to SYSTEM FAILURE LEVEL immediately without fading, unless 'MASK' is stored as the SYSTEM FAILURE LEVEL, in which case the control gear shall stay in the state it is in (no change of the arc power level, no switching on or off).

If the pointer control register CONTROL 254 contains a value other than 0, then the contents of the SYSTEM FAILURE LEVEL shall be used as pointer to the starting point of a sequence. If the pointer control register CONTROL 254 contains 'MASK', the control gear shall run through the sequence until stopped by command. Otherwise, the number of times the gear runs through the sequence shall be given by the contents of CONTROL 254.

On restoration of the idle voltage the control gear shall not change its state.

*Addition:*

### 9.9 Multi-channel device

A sequencer based on this standard shall be able to support up to 8 output channels. Which channels are supported can be queried by command 243 'QUERY SUPPORTED CHANNELS'.

Any direct or indirect arc power control command defined in Part 102 shall influence the arc power level of the selected channels

For configuration of the sequencer, the different channels shall be selected by command 230 'STORE DTR AS CHANNEL SELECTION'. Each bit of the byte CHANNEL SELECTION shall correspond to one output channel:

| | | |
|---|---|---|
| bit 0 | channel 0 selected | '0' = No |
| bit 1 | channel 1 selected | '0' = No |
| bit 2 | channel 2 selected | '0' = No |
| bit 3 | channel 3 selected | '0' = No |
| bit 4 | channel 4 selected | '0' = No |
| bit 5 | channel 5 selected | '0' = No |
| bit 6 | channel 6 selected | '0' = No |
| bit 7 | channel 7 selected | '0' = No |

The CHANNEL SELECTION shall not influence the recall of already stored points.

The following notation is used to refer to a particular point for a particular channel:

Point (point number; channel number)

### 9.10 Sequencer operation

#### 9.10.1 General

Two operating modes shall be supported:

- externally driven sequencer mode;
- automatic sequencer mode.

#### 9.10.2 Externally driven sequencer mode

In this mode, a control device may use the commands 232 'Go To Point N', 233 'Go To Next Point' and 234 'Go To Previous Point' to control the sequence. The arc power level shall be set to the value stored for the recalled point N using the programmed Sequencer Fade Time of the point N.

#### 9.10.3 Automatic sequencer mode

##### 9.10.3.1 Sequencer programming

For each point of the sequencer, the following values shall be stored: a hold time, a sequencer fade time and up to eight arc power levels, one for each channel.

For Point 0 to Point 15, which are identical to Scene 0 to Scene 15, for Point 253 (Power-On) and for Point 254 (System Failure) an additional pointer control register shall be stored. Table 1 gives an overview of the stored variables and the value of the DTR2 used to access the variables.



**Table 1 – Access to the sequencer variables**

| DTR 2 value | Channel | | | | Sequencer fade time | Hold time | Pointer control register |
|---|---|---|---|---|---|---|---|
| | 0 | 1 | ... | n | | | |
| 0 | point (0,0) | point (0,1) | ... | point (0,n) | FT point 0 | HT point 0 | Control 0 |
| 1 | point (1,0) | point (1,1) | ... | point (1,n) | FT point 1 | HT point 1 | Control 1 |
| 2 | point (2,0) | point (2,1) | ... | point (2,n) | FT point 2 | HT point 2 | Control 2 |
| 3 | point (3,0) | point (3,1) | ... | point (3,n) | FT point 3 | HT point 3 | Control 3 |
| 4 | point (4,0) | point (4,1) | ... | point (4,n) | FT point 4 | HT point 4 | Control 4 |
| 5 | point (5,0) | point (5,1) | ... | point (5,n) | FT point 5 | HT point 5 | Control 5 |
| 6 | point (6,0) | point (6,1) | ... | point (6,n) | FT point 6 | HT point 6 | Control 6 |
| 7 | point (7,0) | point (7,1) | ... | point (7,n) | FT point 7 | HT point 7 | Control 7 |
| 8 | point (8,0) | point (8,1) | ... | point (8,n) | FT point 8 | HT point 8 | Control 8 |
| 9 | point (9,0) | point (9,1) | ... | point (9,n) | FT point 9 | HT point 9 | Control 9 |
| 10 | point (10,0) | point (10,1) | ... | point (10,n) | FT point 10 | HT point 10 | Control 10 |
| 11 | point (11,0) | point (11,1) | ... | point (11,n) | FT point 11 | HT point 11 | Control 11 |
| 12 | point (12,0) | point (12,1) | ... | point (12,n) | FT point 12 | HT point 12 | Control 12 |
| 13 | point (13,0) | point (13,1) | ... | point (13,n) | FT point 13 | HT point 13 | Control 13 |
| 14 | point (14,0) | point (14,1) | ... | point (14,n) | FT point 14 | HT point 14 | Control 14 |
| 15 | point (15,0) | point (15,1) | ... | point (15,n) | FT point 15 | HT point 15 | Control 15 |
| 16 | point (16,0) | point (16,1) | ... | point (16,n) | FT point 16 | HT point 16 | |
| 17 | point (17,0) | point (17,1) | ... | point (17,n) | FT point 17 | HT point 17 | |

| DTR 2 value | Channel | | | | Sequencer fade time | Hold time | Pointer control register |
|---|---|---|---|---|---|---|---|
| | 0 | 1 | … | n | | | |
| … | … | … | … | … | … | … | … |
| 249 | point (249,0) | point (249,1) | … | point (249,n) | FT point 249 | HT point 249 | |
| 250 | | | | | | | |
| 251 | | | | | | | |
| 252 | | | … | | | | |
| 253 | point (253,0) | point (253,1) | … | point (253,n) | FT point 253 | HT point 253 | Control 253 |
| 254 | point (254,0) | point (254,1) | … | point (254,n) | FT point 254 | HT point 254 | Control 254 |
| 255 | | | … | | | | |

NOTE Care has to be taken when programming pointers to avoid infinite loops without any change of light output.

#### 9.10.3.2 Sequence programming example

The automatic sequencer mode is explained by means of the following example.

It shall be possible to store more than one sequence in the memory of the control gear. 'MASK' (255) stored in point (N;0) shall specify the point (N-1) as the end point of a sequence. Point N separates the different sequences from each other. Table 2 shows a programming example.

**Table 2 – Sequencer programming example**

| Point number N | Level point (N;0) | |
|---|---|---|
| 0 | 254 | |
| 1 | 200 | |
| 2 | 180 | |
| … | … | |
| A | 120 | End point of sequence 1 |
| A + 1 | 255 | |
| A + 2 | 0 | |
| … | … | |
| B - 1 | 240 | |
| B | 254 | End point of sequence 2 |
| B + 1 | 255 | |
| … | | |

Starting a sequence at any point between Point 0 and Point A shall cause the sequencer to run sequence 1 beginning at the specified starting point. After Point A, the sequence shall always continue at Point 0. Selecting Point (A+1) as starting point shall cause the sequencer to start at point 0.

Starting a sequence at any point between Point (A+2) and Point B shall cause the sequencer to run sequence 2 beginning at the specified starting point. After Point B, the sequence shall always continue at Point (A+2). Selecting Point (B+1) as starting point shall cause the sequencer to start at point (A+2).

Figure 1 shows a timing example for an automatic sequence.

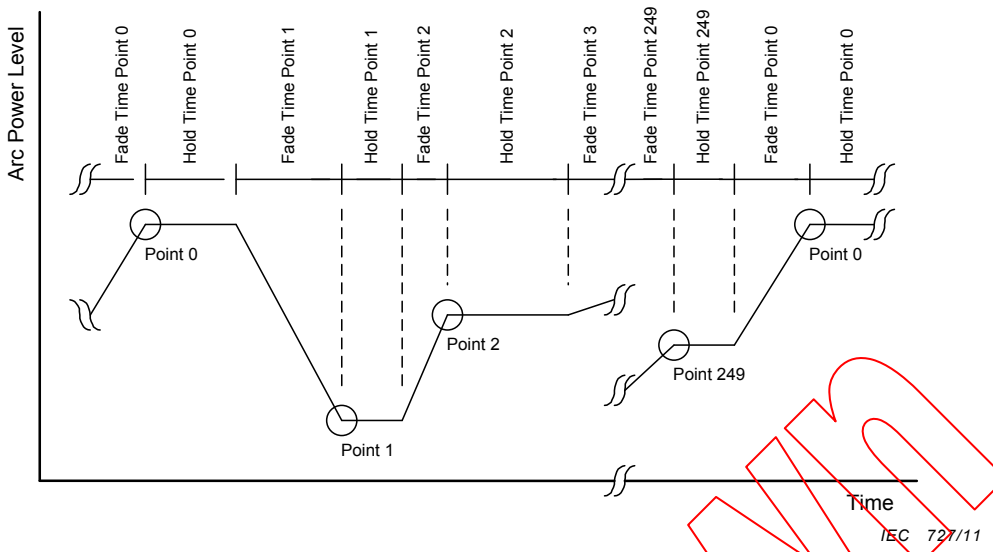


**Figure 1 – Timing example for an automatic sequence**

### 9.10.3.3 Starting the automatic sequencer

#### 9.10.3.3.1 Starting with sequencer commands

To start the automatic sequencer with sequencer commands, the following steps are to be executed by a control device:

a) transmit the starting point to DTR2 and the desired number of loops to DTR;

b) start the sequence with command 235 'START AT POINT N'.

After step b), the control gear shall set the actual level to the level stored for the selected point N using the programmed sequencer fade time of the point N. The actual level shall then remain constant at the programmed value of point N for the configured hold time of point N. After that the sequencer shall operate as described in 9.10.3.1.

#### 9.10.3.3.2 Starting with pointer

On power-up, on interface failure, or on scene recall, the control gear shall check the contents of the appropriate pointer control register.

If the pointer control register checked contains 0, the gear shall go to the stored arc power level as requested, i.e. POWER ON LEVEL, SYSTEM FAILURE LEVEL or SCENE X.

If the pointer control register checked contains a value other than 0, then the contents of the POWER ON LEVEL, SYSTEM FAILURE LEVEL or SCENE X shall be used as pointer to the starting point of a sequence. If the pointer control register contains 'MASK', the control gear shall run through the sequence until stopped by command. Otherwise, the number of times the gear runs through the sequence shall be given by the contents of the pointer control register.

If a pointer points to a non-existent point it shall be ignored and no sequence shall be started.

### 9.10.3.4 Stopping the automatic sequencer

A running automatic sequence shall be stopped on any of the following events:

- the starting of an automatic sequence via pointer;
- the starting of an automatic sequence by command 235 'START AT POINT N';