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INTERNATIONAL STANDARD

NORME INTERNATIONALE

Electrostatics –
Part 4-8: Standard test methods for specific applications – Discharge shielding – Bags

Électrostatique –
Partie 4-8: Méthodes d'essai normalisées pour des applications spécifiques – Blindage contre les décharges – Sacs

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FOREWORD

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International Standard IEC 61340-4-8 has been prepared by IEC technical committee 101: Electrostatics.

The text of this standard is based on ANSI/ESD STM11.31-2006. It was submitted to the National Committees for voting under the Fast Track Procedure.

This bilingual version (2011-04) replaces the English version.

The text of this standard is based on the following documents:

FDIS	Report on voting
101/293/FDIS	101/297/RVD

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

The French version of this standard has not been voted upon.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

A list of all parts in the IEC 61340 series, under the general title *Electrostatics*, can be found on the IEC website.

The committee has decided that the contents of this publication will remain unchanged until the stability date indicated on the IEC web site under "http://webstore.iec.ch" in the data related to the specific publication. At this date, the publication will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

INTRODUCTION

It is the intent of this part of IEC 61340 to provide industry with a common, repeatable method for testing and determining the shielding abilities of electrostatic shielding bags.

This test method improved upon the existing industry test method for static shielding by controlling some of the variables that were not previously addressed such as:

– discharge waveform characteristics;

– capacitive probe capacitance;

– bag size.

This test method has also made a significant change by discontinuing the use of two voltage probes and incorporating a single current probe for measurement purposes. This was done to eliminate the problems that were encountered with attempting to balance the voltage probes which resulted in measurement errors.

ELECTROSTATICS –

Part 4-8: Standard test methods for specific applications – Discharge shielding – Bags

1 Scope

This part of IEC 61340 provides a test method for evaluating the performance of electrostatic discharge shielding bags. The design voltage for the test apparatus is 1 000 V.

The purpose of this standard is to ensure that testing laboratories who use this test method to evaluate a given packaging material will obtain similar results.

2 Normative references

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

ANSI/ESD STM5.1, *ESD association standard test method for electrostatic discharge sensitivity testing – Human body model (HBM) – Component level*[1]

ASTM D-257-78 *(reapproved 1983), Standard test method for DC resistance or conductance of insulating materials*[2]

3 Terms and definitions

For the purposes of this document, the following terms and definitions apply.

3.1
electrostatic shield
barrier or enclosure that limits the penetration of an electrostatic field

3.2
electrostatic discharge shield
barrier or enclosure that limits the passage of current and attenuates an electromagnetic field resulting from an electrostatic discharge

4 Required equipment

4.1 ESD simulator

A basic ESD simulator is shown in Figure 1. This simulator and the resulting waveforms were taken from ANSI/ESD STM5.1. The equivalent circuit for the simulator consists of a 100 pF capacitor in series with a 1 500 Ω resistor.

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1 ESD Association, 7900 Turin Road, Bldg. 3, Ste 2, Rome, NY 13440-2069, 315-339-6937, www.esda.org

2 American Society for Testing and Materials (ASTM) 1916 Race Street, Philadelphia, PA 19103-1187, 215-299-5400

4.2 Waveform verification equipment

Equipment capable of verifying the pulse waveforms defined in this part shall include, but is not limited to, a storage oscilloscope, a high voltage resistor and a suitable current probe.

4.2.1 Oscilloscope

A digital storage oscilloscope capable of a 200 MHz single shot bandwidth and a minimum sampling rate of 500 MSPS.

4.2.2 Current probe

The current probe shall have a minimum frequency response of 500 MHz. Included in the current probes that meet this requirement are a Tektronix CT-1, CT-2 and CT-6. The maximum cable length shall be 1 m.

4.2.3 High voltage resistor

The resistor shall be a 500 Ω, 1 % tolerance, 1 000 V, low inductance, sputtered metal film (Caddock Industries type MG or equivalent).

4.3 Capacitive probe

A parallel plate capacitive probe shall be constructed as shown in Figure 2. The capacitance for the probe shall be 8 pF ± 2 pF. The probe capacitance can be verified according to Clause 6, point c).

The spacer between the plates shall be made of an insulating material such as polycarbonate or acrylic.

4.4 Discharge electrode and ground electrode

The discharge electrode and the ground electrode shall be 3,8 cm ± 0,025 cm (1,5" ± 0,010") in diameter and shall be made of a conductive material. The support area that surrounds the ground electrode should be 20 cm × 25 cm (8" × 10") and have a surface resistivity greater than 1 Ω × 10^{13} Ω per square as measured by ASTM D257-78.

4.5 Bag size

The bags used for this test should be 20 cm × 25 cm (8" × 10" with 20 cm (8") being the open end.

NOTE If other bag sizes are used, care must be taken to ensure that the same size bag is used to provide consistent and fair comparison of bags from various manufacturers. Bags, which are not large enough to have the capacitive probe completely inside the bag may yield erroneous results. Bags with substantial differences in thickness may yield results that do not correlate due to the increased transmission length through the bag.

4.6 Computer/software

A computer should be used to analyse the data that is acquired by the oscilloscope. A generic description of the analysis system is described in Annex A.

4.7 Environmental chamber

A chamber is required that can meet the following environmental test conditions:

– control humidity to 12 % RH ± 3% RH at a temperature of 23° C ± 2° C (73° F ± 3° F);

– control humidity to 50 % RH ± 5% RH at a temperature of 23° C ± 2° C (73° F ± 3° F).

5 ESD simulator waveform verification procedure

The following procedure shall be used to verify the resistive current (*I*p) waveform from the ESD simulator.

a) Connect the 500 Ω resistor specified in 4.2.3 to the wiring from the ESD simulator discharge and ground connections keeping the cabling as short as possible (the cables used should be the same as those used to perform the shielding test). Connect the current probe around the wire end of the resistor which is connected to the ESD simulator ground. Connect the discharge electrode cable to the tester output and the ground electrode cable to equipment ground.

NOTE The conductive discharge and ground electrodes are not used for this portion of the test.

b) Connect the current probe to the storage oscilloscope. Set the scope input resistance to 50 Ω. (Match the impedance of the probe and the scope input.)

c) Set the ESD simulator discharge voltage to 1 000 V.

d) Set the horizontal time scale in the oscilloscope to 5 ns per division and initiate a pulse. Observe the waveform rise time, peak current and leading edge ringing. All parameters shall be within the limits specified in Figure 3a and Clause 5, point 3).

e) If necessary, adjust the ESD simulator voltage level until a peak current (*I*p) of 0,50 A ± 10 % is obtained. This voltage level represents an equivalent 1 000 V discharge level. This is the voltage level that will be used in Clause 7.

f) Set the horizontal time scale in the oscilloscope to 100 ns per division and observe the complete current waveform. The pulse shall meet the decay time requirement (t_d) as shown in Figure 3b.

g) Using the computer analyse the resulting current waveform. The software shall be capable of calculating energy for different resistances. For this portion of the procedure the resistance is 2 000 Ω (this consists of the 1 500 Ω ESD simulator resistance and the 500 Ω high-voltage resistor). The energy from a 1 000 V (100 pF) discharge shall be 50 µJ (± 6 µJ). This is obtained from the equation $E = 1/2\ CV^2$.

6 System verification procedure

a) Connect the 500 Ω resistor between the two conductive plates of the capacitive probe. Place the capacitive probe between the discharge and ground electrodes. Ensure that the discharge electrode, the capacitive probe and the ground electrode are vertically aligned and that there is good contact between all three elements.

b) Connect the current probe to the storage oscilloscope. Set the scope input resistance to 50 Ω.

c) Set the horizontal time scale in the oscilloscope to 5 ns per division and initiate a 1 000 V pulse. The peak current, due to the capacitive loading of the capacitive probe, shall not reduce the peak current to less than 0,42 A due to the capacitance of the capacitive probe.

NOTE If the reading is outside of this range, check the capacitance of the capacitive probe with a capacitance meter and/or adjust the length of the wiring if necessary.

7 Test procedure/conditioning

The test procedure shall be as follows:

a) Place a minimum of six samples of the product to be tested in an environmental chamber set for the following conditions:

- temperature: 23 °C ± 2 °C (73 °F ± 3 °F)
- relative humidity: (12 ± 3) % RH
- conditioning period: minimum of 48 h

Place an equal number of additional samples into an environmental chamber set for the following conditions:

- temperature: 23 °C ± 2 °C (73 °F ± 3 °F)
- relative humidity: (50 ± 3) % RH
- conditioning period: minimum of 48 h.

NOTE All testing to be performed in the conditioned environment.

b) Place the capacitive probe into the 20 cm × 25 cm (8" × 10" bag such that it is 10 cm (4") inside the bag opening and is centered, side to side. Insure good contact between the electrodes, the bag and the probe. If other bag sizes are used, the capacitive probe is to be placed in the geometric centre of the bag.

c) Set the oscilloscope horizontal time scale to 50 ns per division. The horizontal time scale may have to be adjusted if the entire current waveform is not displayed on the oscilloscope.

d) Initiate a 1 000 V pulse (or 1 000 V equivalent) as determined in Clause 5, point e).

e) If using a computer, calculate and record the energy seen inside the bag (use 500 Ω for the resistance setting for the software). Repeat step d) five more times to obtain six data points per bag.

f) Repeat steps b) through e) for the remaining five samples.

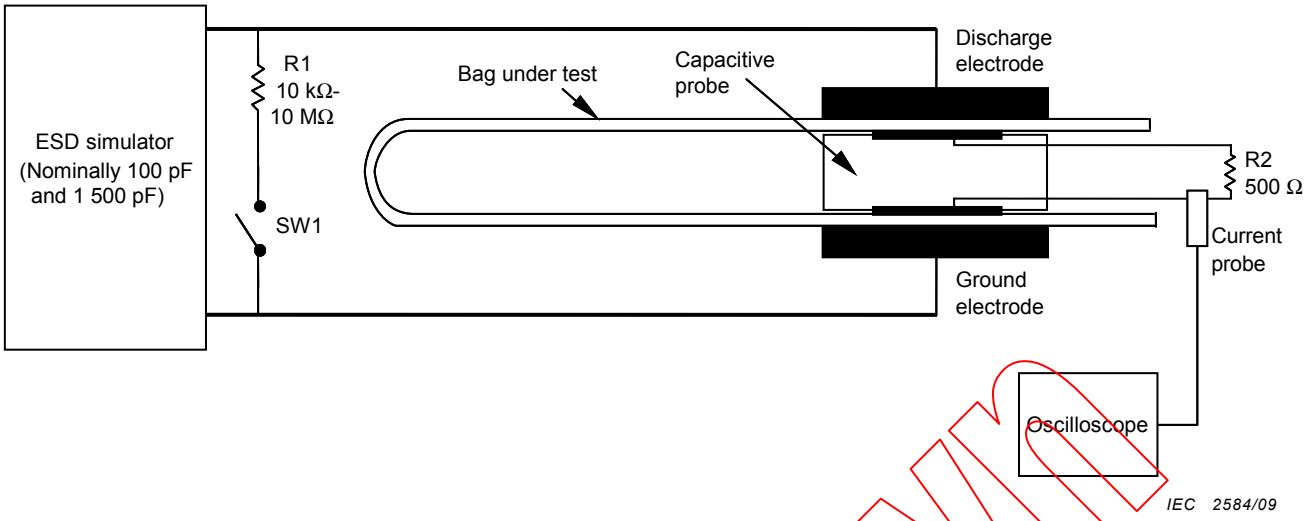
g) Repeat steps b) through f) for the bags that were conditioned at 50 % RH.

8 Reporting

a) Report the average, minimum, maximum and standard deviation of the 36 energy readings for both humidity levels.

b) Record the following extra information:

- peak current;
- bag size;
- bag thickness;
- conditioning period;
- test conditions;
- ESD simulator description (make/model/serial/number);
- scope, producer/model number and last calibration date.



NOTE 1 The current probe is specified in 4.2.2.

NOTE 2 The 500 Ω resistor (R2) is specified in 4.2.3.

NOTE 3 Switch SW1 is closed 10 ms to 100 ms after the pulse delivery period to ensure that the discharge electrode is not left in a charged state. The switch should be open at least 10 ms prior to the delivery of the next pulse. R1 and SW1 are part of the ESD simulator's internal circuitry.

NOTE 4 The performance of the tester is strongly influenced by parasitic capacitance and inductance.

Figure 1 – ESD simulator