INTERNATIONAL STANDARD

IEC 60191-6-5

First edition
2001-08

Mechanical standardization of semiconductor devices –

Part 6-5: General rules for the preparation of outline drawings of surface mounted semiconductor device packages – Design guide for fine-pitch ball grid array (FBGA)

Normalisation mécanique des dispositifs à semiconducteurs

Partie 6-5:
Règles générales pour la préparation des dessins d'encombrement des dispositifs à semiconducteurs à montage en surface –
Guide de conception pour les boîtiers matriciels à billes et à pas fins (FBGA)

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MECHANICAL STANDARDIZATION OF SEMICONDUCTOR DEVICES –

Part 6-5: General rules for the preparation of outline drawings of surface mounted semiconductor device packages – Design guide for fine-pitch ball grid array (FBGA)

FOREWORD

1) The IEC (International Electrotechnical Commission) is a worldwide organization for standardization comprising all national electrotechnical committees (IEC National Committees). The object of the IEC is to promote international co-operation on all questions concerning standardization in the electrical and electronic fields. To this end and in addition to other activities, the IEC publishes International Standards. Their preparation is entrusted to technical committees; any IEC National Committee interested in the subject dealt with may participate in this preparatory work. International, governmental and non-governmental organizations liaising with the IEC also participate in this preparation. The IEC collaborates closely with the International Organization for Standardization (ISO) in accordance with conditions determined by agreement between the two organizations.

2) The formal decisions or agreements of the IEC on technical matters express, as nearly as possible, an international consensus of opinion on the relevant subjects since each technical committee has representation from all interested National Committees.

3) The documents produced have the form of recommendations for international use and are published in the form of standards, technical specifications, technical reports or guides and they are accepted by the National Committees in that sense.

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6) Attention is drawn to the possibility that some of the elements of this International Standard may be the subject of patent rights. The IEC shall not be held responsible for identifying any or all such patent rights.

International Standard IEC 60191-6-5 has been prepared by subcommittee 47D: Mechanical standardization of semiconductor devices, of IEC technical committee 47: Semiconductor devices.

The text of this standard is based on the following documents:

FDIS	Report on voting
47D/437/FDIS	47D/455/RVD

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 3.

The committee has decided that the contents of this publication will remain unchanged until 2003. At this date, the publication will be

- reconfirmed;
- withdrawn;
- replaced by a revised edition; or
- amended.

A bilingual version of this publication may be issued at a later date.

MECHANICAL STANDARDIZATION OF SEMICONDUCTOR DEVICES –

Part 6-5: General rules for the preparation of outline drawings of surface mounted semiconductor device packages – Design guide for fine-pitch ball grid array (FBGA)

1 Scope

This part of IEC 60191 provides common outline drawings and dimensions for all types of structures and composed materials of fine-pitch ball grid array (hereinafter called FBGA), whose terminal pitch is less than, or equal to, 0,80 mm and whose package body outline is square.

The demand for area array style packages exists according to the multi-functioning and high performance of electrical equipment. The object of this design guide is to standardize outlines and secure interchangeability of FBGA packages. The terminal pitch and package outlines of these fine-pitch array packages are smaller than those of BGA packages.

2 Normative references

The following normative documents contain provisions which, through reference in this text, constitute provisions of this part of IEC 60191. For dated references, subsequent amendments to, or revisions of, any of these publications do not apply. However, parties to agreements based on this part of IEC 60191 are encouraged to investigate the possibility of applying the most recent editions of the normative documents indicated below. For undated references, the latest edition of the normative document referred to applies. Members of IEC and ISO maintain registers of currently valid International Standards.

IEC 60191-6:1990, *Mechanical standardization of semiconductor devices – Part 6: General rules for the preparation of outline drawings of surface mounted semiconductor device packages*

3 Definitions

For the purposes of this part of IEC 60191, the definitions contained in IEC 60191-6 as well as the following definitions apply.

3.1
flanged type
type whose package body size (body length and width) consists of its own flange which is composed around the encapsulation or lid

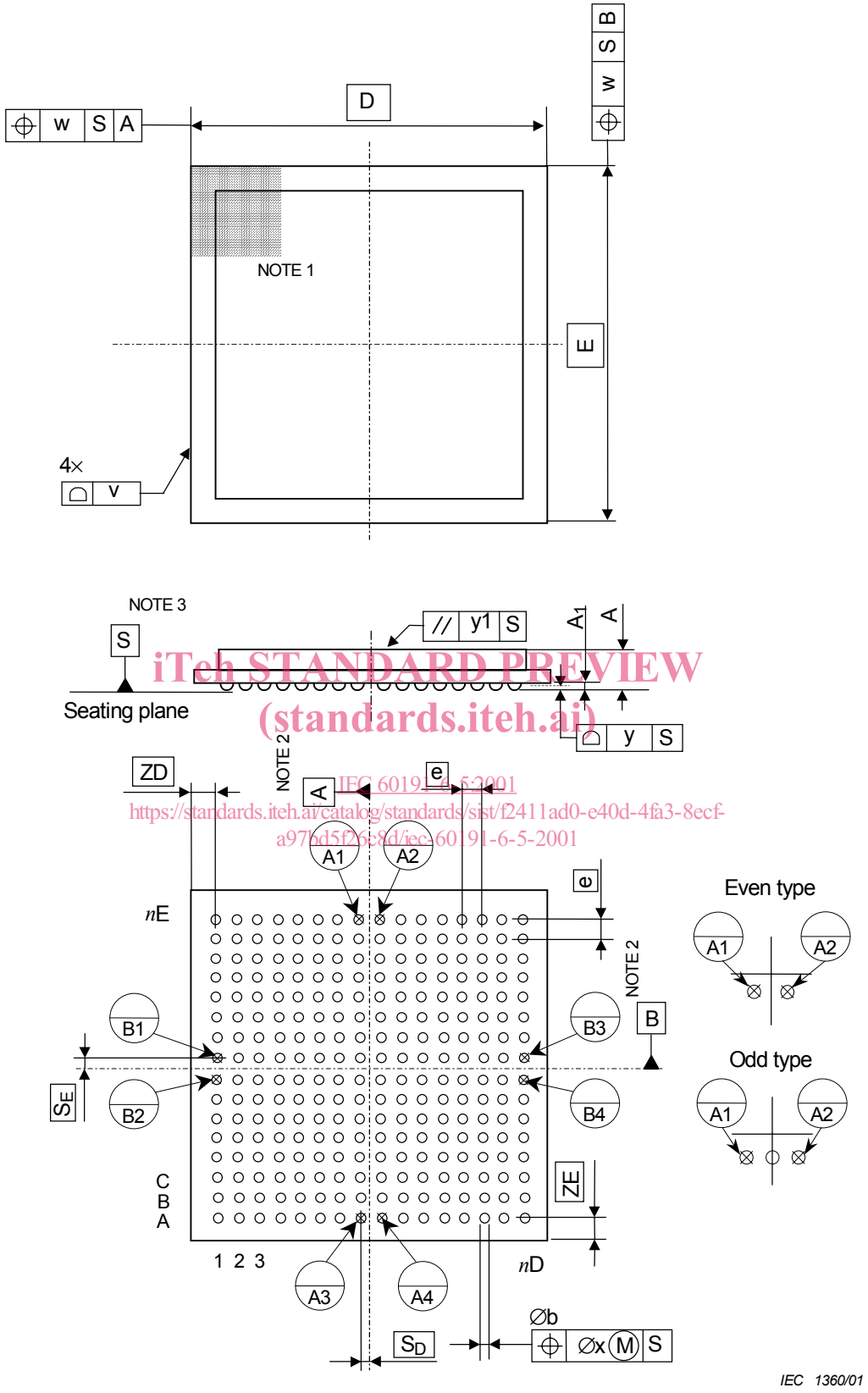
3.2
type of real chip size
type whose package body size (body length and width) consists of an encapsulation just around the real chip only

3.3
fine-pitch ball grid array (FBGA)
packages with metal balls whose terminal pitch is less than, or equal to, 0,80 mm positioned in an array on the base plane of the package as external terminals. This package structure makes it possible to surface-mount the packages to the printed circuit board

3.4
material designation
FBGA packages are classified according to the following two material designations:

3.4.1
plastic type (P-FBGA)
plastic-type classification is assigned to packages which consist of resin substrate as interposer material (e.g. glass-epoxy, polyimid)

3.4.2
ceramic type (C-FBGA)
ceramic-type classification is assigned to packages which consist of ceramic substrate as interposer material



NOTE 1 Zone of a visible index on the top surface.

NOTE 2 Datum A and B are the axes defined by the terminal positions indicated with datum targets.

NOTE 3 Primary datum S and seating plane to be defined by the method of least squares of spherical crowns of land.

Table 1 – Group 1: Dimensions appropriate to mounting and interchangeability

Ref.	Limits to be observed			Recommended values for the dimensions mm	Note
	Min.	Nom.	Max.		
n		X			1, 2
*n*D *n*E		X X			
A			X	A max. = 1,20, 1,70, 2,00	Includes heat slug Includes package warpage and tilt
A1	X	X	X	Min. Nom. Max. at e = 0,80 0,35 0,40 0,45 at e = 0,65 0,28 0,33 0,38 at e = 0,50 0,20 0,25 0,30 at e = 0,40 0,15 0,20 0,25	
øb	X	X	X	Min. Nom. Max. at e = 0,80 0,45 0,50 0,55 at e = 0,65 0,35 0,40 0,45 at e = 0,50 0,25 0,30 0,35 at e = 0,40 0,20 0,25 0,30	
D		X		At flanged type D = 4,0, 5,0, 6,0, 7,0, 8,0, 9,0, 10,0, 11,0, 12,0, 13,0, 14,0, 15,0, 16,0, 17,0, 18,0, 19,0, 20,0, 21,0 at type of real chip size D = from 3,1 to 21,0	Dimension range shows nominal value
E		X		at flanged type E = 4,0, 5,0, 6,0, 7,0, 8,0, 9,0, 10,0, 11,0, 12,0, 13,0, 14,0, 15,0, 16,0, 17,0, 18,0, 19,0, 20,0, 21,0 at type of real chip size E = from 3,1 to 21,0	Dimension range shows nominal value
e		X		e = 0,80, 0,65, 0,50, 0,40	
v			X	v = 0,15	Includes burrs
w			X	at e = 0,80 w = 0,20 at e = 0,65 w = 0,20 at e = 0,50 w = 0,20 at e = 0,40 w = 0,15	
x			X	at e = 0,80 x = 0,08 at e = 0,65 x = 0,08 at e = 0,50 x = 0,05 at e = 0,40 x = 0,05	