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INTERNATIONAL STANDARD

NORME INTERNATIONALE

Electrostatic discharge sensitivity testing – Transmission line pulse (TLP) – Component level

Essai de sensibilité aux décharges électrostatiques – Impulsion de ligne de transmission (TLP) – Niveau composant

IEC 62615:2010

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ELECTROSTATIC DISCHARGE SENSITIVITY TESTING – TRANSMISSION LINE PULSE (TLP) – COMPONENT LEVEL

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International Standard IEC 62615 has been prepared by IEC technical committee 47: Semiconductor devices.

This first edition is based on an ANSI/ESDA document ANSI/ESD STM5.5.1-2008.

The text of this standard is based on the following documents:

FDIS	Report on voting
47/2046/FDIS	47/2056/RVD

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

The committee has decided that the contents of this publication will remain unchanged until the stability date indicated on the IEC web site under "http://webstore.iec.ch" in the data related to the specific publication. At this date, the publication will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

INTRODUCTION

Interest in TLP testing is growing rapidly in the testing of electronic components in the semiconductor industry. TLP testing techniques are being used for semiconductor process development, device and circuit design. This technique or practice is being utilized on products in both wafer level and packaged environments. TLP testing is used as an electrostatic discharge (ESD) characterization tool to obtain voltage-current pulse characterization parameters, failure levels, and ESD metrics. The TLP technique is being used today as a standard measurement for ESD devices. The TLP system to the ESD engineer is becoming a tool as critical as the 'parameter analyzer' is to the semiconductor engineer.

The majority of TLP systems are designed by engineers in a laboratory environment. A number of commercial TLP systems have been marketed in the industry. Hence it is clear a TLP specification was needed for the TLP vendors, semiconductor industry and product customers to be able to make valid data comparisons. With the usage of TLP data for ESD characterization, technology benchmarking, and product quality evaluation, there is a growing need to have standard methodologies, failure criteria, and means of reporting to allow dialogue between semiconductor suppliers, vendors, and product customers.

This document defines the standard test method used today in the semiconductor industry for TLP testing method and techniques in both industrial and academic institutions (this document is intended to be used by electrical technicians, electrical engineers, semiconductor process and device engineers, ESD reliability and quality engineers, and circuit designers).

The context of this document is the application of TLP techniques for the electrical characterization of semiconductor components. These semiconductor components can be single devices, a plurality of devices, integrated circuits, or semiconductor chips. This methodology is relevant to both active and passive elements. This test method is applicable to diodes, MOSFET devices, bipolar transistors, resistors, capacitors, inductors, contacts, vias, wire interconnects, and related components.

ELECTROSTATIC DISCHARGE SENSITIVITY TESTING – TRANSMISSION LINE PULSE (TLP) – COMPONENT LEVEL

1 Scope and object

This International Standard defines a method for pulse testing to evaluate the voltage current response of the component under test and to consider protection design parameters for electro-static discharge (ESD) human body model (HBM). This technique is known as transmission line pulse (TLP) testing.

This document establishes a methodology for both testing and reporting information associated with transmission line pulse (TLP) testing. The scope and focus of this document pertains to TLP testing techniques of semiconductor components.

This document should not become alternative method of HBM test standard such as IEC 60749-26. The purpose of the document is to establish guidelines of TLP methods that allow the extraction of HBM ESD parameters on semiconductor devices. This document provides the standard measurement and procedure for the correct extraction of HBM ESD parameters by using TLP.

2 Normative references

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60749-26: *Semiconductor devices – Mechanical and climatic test methods – Part 26: Electrostatic discharge (ESD) sensitivity testing – Human body model (HBM)*

IEC 60749-27, *Semiconductor devices – Mechanical and climatic test methods – Part 27: Electrostatic discharge (ESD) sensitivity testing – Machine model (MM)*

IEC 60749-28, *Semiconductor devices – Mechanical and climatic test methods – Part 28: Electrostatic discharge (ESD) sensitivity testing – Direct contact charged device model (DC-CDM)*[1]

3 Terms and definitions

For the purposes of this document, the following terms and definitions apply.

3.1
current source method
TLP methodology (sometimes referred to as constant current method) that utilizes a 500 Ω resistor in series with the DUT and measures the voltage and current at the DUT

3.2
destructive damage
damage where the operating electrical characteristics or parameters are altered and do not recover to the initial conditions prior to stress

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1 *Under consideration.*

3.3
safe operation area
(SOA)
current and voltage regime where a device is in normal operation without degradation

3.4
second breakdown
condition where a negative resistance state occurs in a device due to thermal processes

NOTE This is designated as the voltage trigger point V_{t2} and current I_{t2}. and is typically observed after electrical breakdown (e.g., V_{t1}, I_{t1})

3.5
thermal instability
condition whereby a device is in a negative resistance regime due to thermal processes

3.6
time domain reflectometer method
(TDR)
TLP methodology that uses an oscilloscope to measure both the incident and the reflected waves from the device under test (DUT)

3.7
time domain transmission method
(TDT)
TLP methodology that uses an oscilloscope to measure the transmitted wave after application to the device under test (DUT)

3.8
time domain transmission and reflection method
(TDRT)
TLP methodology that incorporates both the transmitted and reflected waves

3.9
transmission line pulse
(TLP)
a rectangular current pulse formed by discharging a charged transmission line cable.

NOTE In this document, TLP refers to any rectangular pulse formed from any pulse source

3.10
transmission line pulse test system
a test system that applies a rectangular pulse to a device under test and allows measurement of device electrical characteristics during a pulsed state

NOTE The system typically measures current and voltage across the device, as well as leakage current after TLP pulse application

4 Test apparatus

4.1 General

Transmission line pulse (TLP) systems vary in their use of equipment, configurations, and methodology to extract the current and voltage characteristics of a device. TLP design and system configuration is contained in Annex A.

All equipment within the test system shall be able to withstand the maximum current for the largest pulse width applied. Additionally, all equipment shall withstand the maximum voltage from the initial charge voltage (including the reflected voltage) observed in the test system. Current and voltage probes shall not saturate and/or fail during TLP testing.

4.2 Oscilloscope

Oscilloscope requirements:

a) minimum single shot bandwidth of at least 500 MHz

4.3 Voltage probe

Voltage probe requirements:

a) a minimum bandwidth of 200 MHz.
b) shall be able to withstand a maximum voltage of twice the open-circuit maximum voltage (e.g. twice the pre-charge voltage) without electrical damage

4.4 Current probe

Current probe requirements:

a) a minimum bandwidth of 1 GHz.
b) shall not saturate under TLP test maximum current and/or maximum pulse width

4.5 Transmission line

Transmission line requirements:

a) shall be able to withstand the maximum current for the largest TLP test pulse width without electrical damage.
b) shall be able to withstand the maximum TLP test voltage observed (combined initial charge voltage and reflected voltage) without electrical damage.

4.6 High voltage power supply

High voltage power supply requirements:

a) shall be able to source TLP test voltage levels required to evaluate the DUT.
b) shall be able to withstand the maximum TLP test voltage observed (combined initial charge voltage and reflected voltage) without electrical damage.

4.7 High voltage switch

High voltage switch requirements:

a) shall be able to withstand maximum current for the largest TLP test pulse width without electrical damage.
b) shall be able to withstand the maximum TLP test voltage observed (combined initial charge voltage and reflected voltage) without electrical damage.

4.8 Attenuator

Attenuator requirements:

a) shall be able to withstand maximum current for the largest TLP test pulse width without electrical damage.
b) shall be able to withstand the maximum TLP test voltage observed (combined initial charge voltage and reflected voltage) without electrical damage.

4.9 Rise time filter

Rise time filter requirements:

a) shall be able to withstand maximum current for the largest TLP test pulse width without electrical damage.

b) shall be able to withstand the maximum TLP test voltage observed (combined initial charge voltage and reflected voltage) without electrical damage.

5 TLP waveform parameters

5.1 Pulse characteristics

This subclause describes pulse characteristics for specified load conditions. Table 1 summarizes these pulse characteristics.

Table 1 – TLP current and voltage pulse parameters

TLP Pulse Parameters (Voltage and Current Conditions)	Typical Value	Load Condition
Current pulse width	100 ns	Short
Voltage rise time	0,2 to 10 ns	Open
Current rise time	0,2 to 10 ns	Short
Fall time	Greater or equal to rise time	N/A
Maximum peak voltage overshoot	20 % of plateau	Open
Maximum voltage ringing duration	25 % of pulse width	Open
Maximum peak current overshoot	20 % of plateau	Short
Maximum current ringing duration	25 % of pulse width	Short
Measurement time window	10 % to 95 % of pulse width	N/A

5.2 Pulse plateau

The pulse plateau is the pulse time-averaged maximum value.

5.3 Pulse width

The pulse width is defined as the full width half maximum or FWHM. The most commonly used TLP pulse width is 100 ns (see Figure 1).

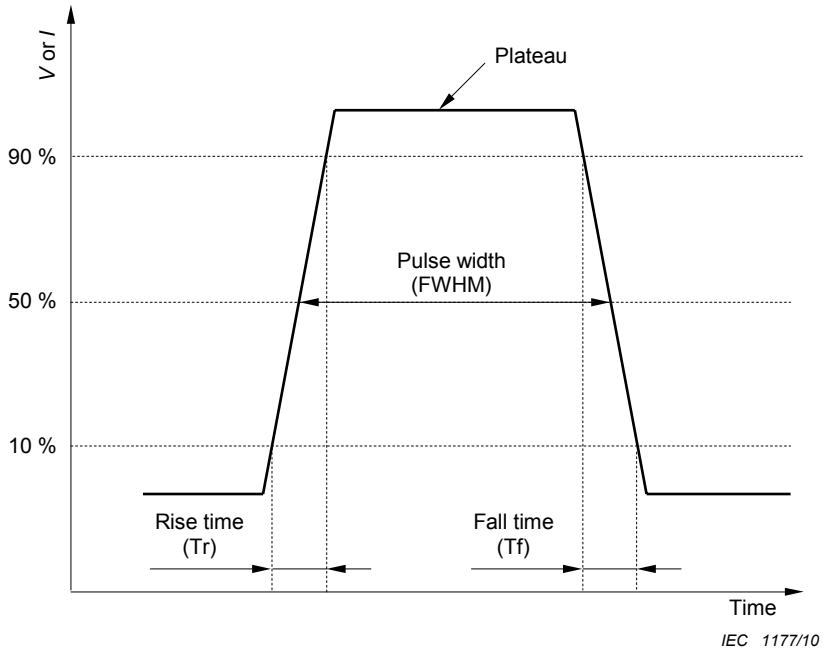

Figure 1 – TLP waveform parameter illustration for pulse width rise time and fall time (parameters apply to both voltage and current TLP waveforms)

5.4 Rise time

Rise time is defined as the time it takes the voltage or current to rise from 10 % to 90 % of the pulse plateau (see Figure 1). TLP systems have a typical rise time of less than 10 ns.

5.5 Fall time

Fall time is defined as the time it takes the voltage or current to decrease from 90 % to 10 % of the pulse plateau (see Figure 1). The fall time shall be equal to or greater than the rise time. When a pulse source other than a charged transmission line is used for pulse generation, it is recommended that the fall time be equal to the rise time.

5.6 Maximum peak current overshoot

The maximum peak current overshoot is defined as the magnitude of the overshoot peak current (into a short circuit) to the current plateau of the measured pulse (see Figure 2). It shall be less than 20 % of the plateau current.

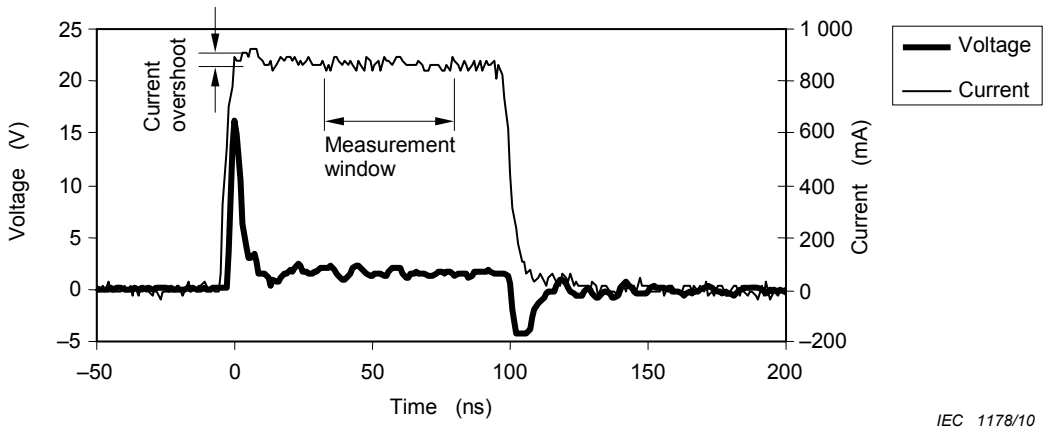

Figure 2 – Illustration of maximum peak current overshoot

5.7 Maximum current ringing duration

The maximum current ringing duration is defined as the duration of time between the beginning of the current pulse and the time that the ringing reaches less than 5 % of the plateau current magnitude. The maximum ringing duration shall be less than 25 % of the pulse width. For example, a 100 ns TLP pulse shall have a maximum ringing duration of less than 25 ns.

5.8 Maximum peak voltage overshoot

The maximum peak voltage overshoot is defined as the magnitude of the overshoot peak voltage to the voltage plateau of the measured pulse (see Figure 3). It shall be less than 20 % of the plateau voltage magnitude.

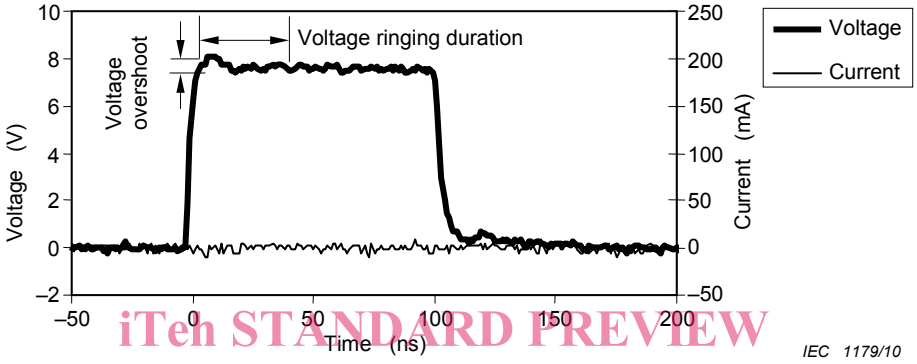

Figure 3 – Illustration of maximum peak voltage overshoot

5.9 Maximum voltage ringing duration

The maximum voltage ringing duration is defined as the length of time between the first overshoot beyond the plateau voltage to the time when it settles to within 5 % of the plateau voltage. The maximum ringing duration shall be less than 25 % of the pulse width. For example, a 100 ns TLP pulse shall have maximum ringing duration of less than 25 ns.

5.10 Measurement window

The measurement window is the range of time within the pulse width where the voltage and current of the device under test (DUT) are measured. The length of the measurement window shall be more than 10 % of the pulse width to achieve accuracy by averaging many data points.

6 Test requirements and procedures

6.1 Error correction

Adjustments of both current and voltage measurements are important to remove unavoidable non-ideal system characteristics such as system resistance, contact resistances, and shunt resistance. Periodic verification using simple components with known properties insures accurate measurements.

6.2 Tester error correction methodology

6.2.1 General methodology

Perform the error correction methodology, including the open and short circuit measurements, at least once per shift or when the equipment is modified or changed. Longer periods between error correction steps may be used if no changes in the error correction factors are observed

for several consecutive checks. Create a separate set of adjustment values for each test pulse rise time, or configuration of cables and probes used to collect device data. The adjustments derived from the short circuit and open circuit measurements may be applied to the data within the operating system software, during post processing using spreadsheet or other data analysis software or can be done manually. To insure accurate results, all measurements shall be performed on properly calibrated measurement instruments.

6.2.2 Error correction short circuit methodology

Measurements through a short circuit allow for correction of system and contact resistance.

Connect an electrical short circuit to the end of the device testing connections or needles at the DUT. In the case of wafer probes, placing probe needles on a low resistance clean metal can be considered as a good electrical short circuit. The short circuit shall be made of the same type of material to be used during device measurements or verification, and shall be verified by standard low resistance measurement techniques with accuracy to 1 mΩ.

Perform a TLP test (see 6.4 for test procedure) with at least 5 points set to the maximum current. If the slope of a line through the test points is not 0 Ω, then the value of the slope of the line in V/I (Ω) represents the internal adjustment value and shall be used to correct the DUT I-V test data.

Record the measured V-/I-values for reference and use until the next short circuit error correction.

For the greatest accuracy, use an I-V plot range of ±1 V with the current range set to highest value used in the TLP system.

6.2.3 Error correction open circuit methodology

Measurements through an open circuit allow the correction of shunt resistance contributions.

Provide an open circuit at the end of the device testing connections for a socket tester. For wafer probing, disconnecting the probe needles from the short circuit will provide an optimum open circuit.

Perform a TLP test (see 6.4 for test procedure) with at least 5 points set to the maximum voltage. If the slope of a line through the test points is not infinite, then the value of the slope of the line represents the internal adjustment value and shall be used to correct the DUT I-V test data.

Record the measured V-/I-values for reference and use until the next open circuit error correction.

For the greatest accuracy, use an I-V plot range of ±10 mA with the voltage range set to the highest value used for device testing.

NOTE Typically the current probe losses inject 1 Ω into the current carrying wire, thus the total V/I correction will be greater than 1 Ω. TLP test leads running to a wafer probe station can add an additional 1 Ω to the V/I error correction. Therefore, the V/I error correction can be approximately 1 Ω for socket testing and 1 Ω to 2 Ω for wafer testing. Unless a voltage probe with a lower resistance provides greater shunt losses, the I/V error correction will vary between 10 kΩ and 100 kΩ.

6.3 Tester verification methodology

Verification of TLP test system accuracy shall be performed on a regular basis and prior to system use to minimize error in the measurements. The verification procedure and methodology is dependent on the TLP method being utilized. Verification is performed using