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INTERNATIONAL STANDARD

NORME INTERNATIONALE

Semiconductor devices – Mechanical and climatic test methods – Part 34: Power cycling

Dispositifs à semiconducteurs – Méthodes d'essais mécaniques et climatiques – Partie 34: Cycles en puissance

IEC 60749-34:2010

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International Standard IEC 60749-34 has been prepared by IEC technical committee 47: Semiconductor devices.

This second edition cancels and replaces the first edition published in 2004 and constitutes a technical revision. The significant changes with respect from the previous edition include:

- the specification of tighter conditions for more accelerated power cycling in the wire bond fatigue mode;
- information that under harsh power cycling conditions high current densities in a thin die metalization might initiate electromigration effects close to wire bonds.

The text of this standard is based on the following documents:

FDIS	Report on voting
47/2068/FDIS	47/2079/RVD

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

A list of all parts in the IEC 60749 series, under the general title *Semiconductor devices – Mechanical and climatic test methods*, can be found on the IEC website.

The committee has decided that the contents of this publication will remain unchanged until the stability date indicated on the IEC web site under "http://webstore.iec.ch" in the data related to the specific publication. At this date, the publication will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

SEMICONDUCTOR DEVICES –
MECHANICAL AND CLIMATIC TEST METHODS –

Part 34: Power cycling

1 Scope and object

This part of IEC 60749 describes a test method used to determine the resistance of a semiconductor device to thermal and mechanical stresses due to cycling the power dissipation of the internal semiconductor die and internal connectors. This happens when low-voltage operating biases for forward conduction (load currents) are periodically applied and removed, causing rapid changes of temperature. The power cycling test is intended to simulate typical applications in power electronics and is complementary to high temperature operating life (see IEC 60749-23). Exposure to this test may not induce the same failure mechanisms as exposure to air-to-air temperature cycling, or to rapid change of temperature using the two-fluid-baths method. This test causes wear-out and is considered destructive.

NOTE It is not the intention of this specification to provide prediction models for lifetime evaluation.

2 Normative references

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60747-1:2006, *Semiconductor devices – Part 1: General*

IEC 60747-2:2000, *Semiconductor devices – Discrete devices and integrated circuits – Part 2. Rectifier diodes*

IEC 60747-6:2000, *Semiconductor devices – Part 6: Thyristors*

IEC 60749-3, *Semiconductor devices – Mechanical and climatic test methods – Part 3: External visual examination*

IEC 60749-23, *Semiconductor devices – Mechanical and climatic test methods – Part 23: High temperature operating life*

3 Terms and definitions

For the purposes of this document the following terms and definitions apply.

NOTE Further terms and definitions concerning semi-conductor devices are contained in the IEC 60747 and IEC 60748 series.

3.1
load current
current to which the devices are subjected to produce power loss P

3.2
case temperature
T_c
temperature of the base of the device under test facing the heat sink

3.3
sink temperature
T_s
temperature of the heat sink measured in close proximity to the device under test

3.4
junction temperature excursion
ΔT_{vj}
difference between maximum and minimum virtual junction temperature of the device under test during one power cycle

3.5
case temperature excursion
ΔT_c
difference between maximum and minimum case temperature during one power cycle

3.6
on-time
time interval while device under test is conducting load current

3.7
power loss
P
power dissipation of the devices under test as calculated from current waveform during on-time and from characteristic data in the procurement documents

3.8
off-time
time interval for cooling down

3.9
cycle period
sum of on-time and off-time

4 Test apparatus

The apparatus required for this test shall consist of heat sinking for a group of devices or alternatively for each individual device under test with the purpose of dissipating the forward conduction losses and of controlling on- and off-times. The heat sinking can be selected from natural or forced air convection or liquid cooling. Pre-selected temperature excursions of the device ground plates and of the die junctions, as well as on- and off-times determine heat sinking set-up and parameters.

Sockets or other mounting means shall be provided so that reliable electrical contact can be made without excessive heat transfer to the device terminals. Power supplies shall be capable of maintaining the specified operating conditions throughout the testing period despite normal variations in line voltage or ambient temperatures. On- and off-switching of load currents should be provided by the test circuit independent of any (gate-) control functions of the devices under test. On- and off-times (cycle period) shall be controlled by monitoring either heat sink T_s or case temperature T_c. Alternatively, the cycle period can also be controlled by fixed time settings, if appropriate.

The test circuit should also be designed so that the existence of abnormal or failed devices does not alter the specified conditions for other units on test (e.g. the latter might be accomplished by exchanging defective units with new ones). Care should be taken to avoid possible damage from transient voltage spikes or other conditions that might result in electrical, thermal or mechanical overstress.

5 Procedure

When special mounting or heat sinking is required, the details shall be specified in the applicable procurement documents. Load current and waveforms shall be selected close to the preferred application of the devices under test, as outlined below.

Rectifier devices such as diodes or SCRs that are normally used as a.c. lines converters should be connected to 50 Hz or 60 Hz a.c. power supplies; bridge rectifiers should be operated as such, i.e. a.c. line voltages applied to the a.c. input terminals and output terminals shorted via shunt resistors to monitor load current.

MOS-controlled devices such as power MOSFETs or IGBTs should be connected to d.c. power supplies.

Modules with multiple functions can be operated stepwise and separate according to their internal circuits.

Gate-controllable devices such as SCRs, IGBTs and MOSFETs should be set into a continuous forward conductive state by appropriate gate controls throughout the entire test duration.

The power should be applied and suitable checks made to assure that all devices are properly biased. During the test, the power applied to the devices shall be alternately cycled as given in Table 1, unless otherwise specified in the relevant specification. The devices shall concurrently be cycled between temperature extremes for the specified number of cycles.

The power cycling test shall be continuous except when parts are removed from the test fixtures for interim electrical measurements. If the test is interrupted as a result of device, power or equipment failure, the test shall restart from the point of stoppage.

6 Test conditions

The test condition shall be selected from those outlined in Table 1. The relationship of on-time to off-time shall be the same for all devices under test. It is sufficient that T_{s} or T_{c} is monitored closely below the centre of one device under test, provided that load and heat sinking conditions are properly controlled for all other devices.

Junction temperatures T_{vj}, junction temperature excursions ΔT_{vj} and case temperature excursions ΔT_{c}, shall be kept within the same range for all devices, as given in Table 1 below. Off-time shall be adjusted until T_{vj} has approached T_{c} within $^{+5}_{\;0}$ °C before a new cycle starts, as illustrated in Figure 1.

Junction temperatures T_{vj} (and case temperatures T_{c} if applicable) shall be calculated from the given thermal impedances in the applicable procurement documents and from the power loss P of the devices under test, taking into account load current waveforms.

The number of cycles N_{c} to be performed shall be selected in integer multiples of

- 100 000 for test condition 1,
- 1 000 for test conditions 2 and 3.

No minimum requirements for N_{c} are defined since this figure is very dependent on the application; N_{c} might be millions of cycles in traction applications under test condition 1.

Table 1 – Test conditions

Test condition	**Temperature extremes**		**Cycle period**	**ΔT_{vj}** °C	**Example of failure mode**
	ΔT_c °C	**T_{vj}** °C			
1a	< 30 [a]	45 (±5) to $125\ (^{\ 0}_{-10})$	1 s to 15 s	60 ± 5	Sensitive to wire bond fatigue [b]
1b		45 (±5) to $150\ (^{\ 0}_{-10})$		80 ± 5	
2	50 (±20)	45 (±5) to $125\ (^{\ 0}_{-10})$	1 min to 15 min	75 ± 5	Sensitive to soft solder [c] and wire bond fatigue
3	60 (±20)	45 (±5) to $150\ (^{\ 0}_{-10})$		95 ± 5	

[a] ΔT_c might be very small because the device is normally operated in transient regime during short cycling.

[b] See [1][1]. Under harsh power cycling conditions high current densities in a thin die metalization might initiate electromigration effects close to wire bonds.

[c] See [2].

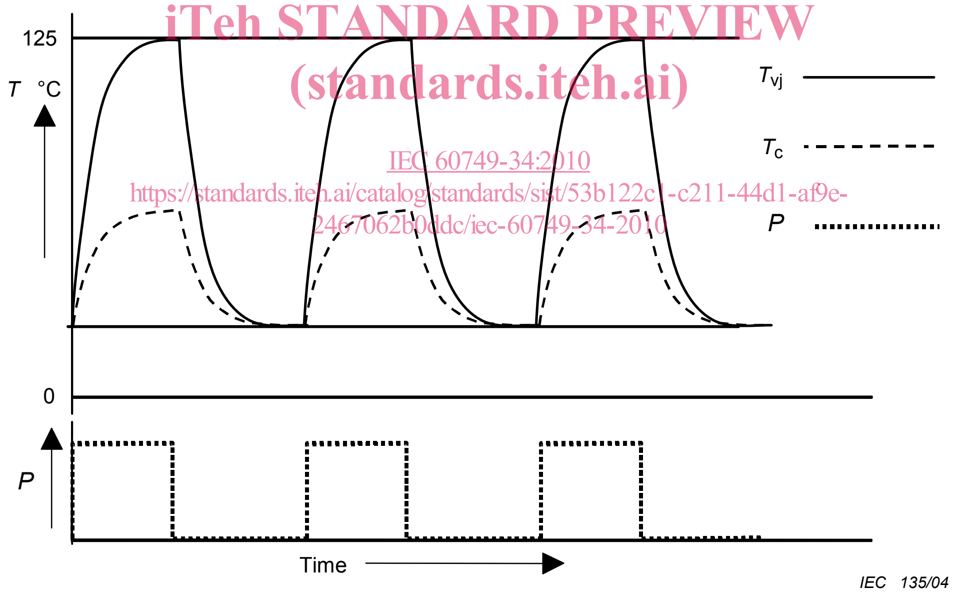

Figure 1 – Typical load power *P* and temperature cycle test condition 2

7 Precautions

Load currents and total power loss shall not exceed specified maximum values per device. The circuit should be structured so that the maximum rated case or junction temperatures shall not be exceeded. Precautions should be taken to avoid electrical damage and thermal runaway. The test set-up should be monitored initially and at the conclusion of a test interval to establish that all devices are being stressed to the specified requirements. Deviations shall be corrected after initial monitoring to assure the validity of the qualification data.

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[1] Figures in square brackets refer to the Bibliography.

8 Measurements

The electrical measurements and visual inspections shall be made at intervals in accordance with the relevant specification.

9 Failure criteria

After exposure to the test, or during the course of the test, a device shall be defined as a failure, if failure-defining characteristics exceed the limits given in 7.2 of IEC 60747-1:2006, with further reference to Table 2 of IEC 60747-2:2000 and Table 3 of IEC 60747-6:2000. Mechanical damage, such as cracking, chipping or breaking of the package (as defined in IEC 60749-3) shall be considered a failure, provided that fixing or handling did not induce such damage.

10 Summary

The following details shall be specified in the relevant specification:

a) special mounting if applicable (see Clause 5);

b) test conditions from Table 1;

c) load current and shape of current (see Clause 7);

d) switch-on time, switch-off time or cycle time, respectively (see Clause 6);

e) number of power cycles to be performed (see Clause 6);

f) for qualification testing, sample size and quality level;

g) interim measurement intervals, when required;

h) electrical measurements (see Clause 8);

i) visual inspection (see Clause 9).