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Integrated circuits – Measurement of impulse immunity – Part 3: Non-synchronous transient injection method

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Circuits intégrés – Mesure de l'immunité aux impulsions – Partie 3: Méthode d'injection de transitoires non synchrones

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INTEGRATED CIRCUITS – MEASUREMENT OF IMPULSE IMMUNITY –

Part 3: Non-synchronous transient injection method

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International Standard IEC 62215-3 has been prepared by subcommittee 47A: Integrated circuits, of IEC technical committee 47: Semiconductor devices.

The text of this standard is based on the following documents:

CDV	Report on voting
47A/881/CDV	47A/890/RVC

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

A list of all parts in the IEC 62215 series, published under the general title *Integrated circuits – Measurement of impulse immunity* can be found on the IEC website.

The committee has decided that the contents of this publication will remain unchanged until the stability date indicated on the IEC web site under "http://webstore.iec.ch" in the data related to the specific publication. At this date, the publication will be

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- withdrawn,
- replaced by a revised edition, or
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INTEGRATED CIRCUITS – MEASUREMENT OF IMPULSE IMMUNITY –

Part 3: Non-synchronous transient injection method

1 Scope

This part of IEC 62215 specifies a method for measuring the immunity of an integrated circuit (IC) to standardized conducted electrical transient disturbances. The disturbances, not necessarily synchronized to the operation of the device under test (DUT), are applied to the IC pins via coupling networks. This method enables understanding and classification of interaction between conducted transient disturbances and performance degradation induced in ICs regardless of transients within or beyond the specified operating voltage range.

2 Normative references

The following documents, in whole or in part, are normatively referenced in this document and are indispensable for its application. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

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IEC 60050 (all parts), *International Electrotechnical Vocabulary (IEV)* (available at <http://www.electropedia.org>)

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IEC 61000-4-4:2012, *Electromagnetic compatibility (EMC) – Part 4-4: Testing and measurement techniques – Electrical fast transient/burst immunity test*

IEC 61000-4-5:2005, *Electromagnetic compatibility (EMC) – Part 4-5: Testing and measurement techniques – Surge immunity test*

IEC 62132-4:2006, *Integrated circuits – Measurement of electromagnetic immunity 150 kHz to 1 GHz – Part 4: Direct RF power injection method*

ISO 7637-2:2011, *Road vehicles – Electrical disturbances from conduction and coupling – Part 2: Electrical transient conduction along supply lines only*

3 Terms and definitions

For the purposes of this document, the terms and definitions given in IEC 60050-131 and IEC 60050-161, some of which have been added for convenience, as well as the following apply.

3.1
auxiliary equipment
equipment not under test but is indispensable for setting up all the functions and assessing the correct performance (operation) of the equipment under test (EUT) during its exposure to the disturbance

3.2
burst
sequence of a limited number of distinct impulses or an oscillation of limited duration

3.3
coupling network
electrical circuit for transferring energy from one circuit to another with well-defined impedance and known transfer characteristics

3.4
performance degradation
undesired departure in the operational performance of any device, equipment or system from its intended performance

Note 1 to entry: The term “degradation” can apply to temporary or permanent failure.

3.5
DUT
device under test
device, equipment or system being evaluated

Note 1 to entry: In this part of IEC 62215, it refers to a semiconductor device being tested.

Note 2 to entry: This note applies to the French language only.

3.6
EMC
electromagnetic compatibility
ability of an equipment or system to function satisfactorily in its electromagnetic environment without introducing intolerable electromagnetic disturbance to anything in that environment

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3.7
global pin
pin that carries a signal or power which enters or leaves the application board without any active device in between

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3.8
immunity
ability of a device, equipment or system to perform without degradation in the presence of an electromagnetic disturbance

3.9
jitter
short-term variations of the significant instants of a digital signal from their ideal positions in time

3.10
local pin
pin that carries a signal or power which does not leave the application board

Note 1 to entry: The signal or power remains on the application board as a signal between two components with or without additional EMC circuitry.

3.11
response signal
signal generated by the DUT for the purpose of monitoring for detecting performance degradation

3.12
electromagnetic ambient
totality of electromagnetic phenomena existing at a given location

3.13
transient
pertaining to or designating a phenomenon or a quantity which varies between two consecutive steady states during a time interval which is short compared with the time-scale of interest

3.14
surge voltage
transient voltage wave propagating along a line or a circuit and characterized by rapid increase followed by a slower decrease of the voltage

3.15
VS
power supply input

3.16
Z_L
line impedance of a trace on the test board

4 General

Electrical transients are a common part of the EMC environment of electrical and electronic devices. These transients are generated often on power nets and are directly applied or coupled to the terminals of integrated circuits which may affect the functionality of the device. The knowledge about the impulse immunity level enables the optimization of the IC as well as the definition of application requirements.

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The transient waveforms are dependent on the application area of the DUT. Typical transient waveforms are burst and surge voltages as specified in IEC 61000-4-4 and IEC 61000-4-5 for industrial and consumer applications and in ISO 7637-2 for automotive application to get reproducible and comparable results for different DUTs.

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The impulse immunity measurement method as described in this standard uses impulses with different amplitude and rise times, duration, energy and polarity in a conductive mode to the IC. In this test method the test time or the number of the applied impulses has to be chosen in a way that statistical effects are covered.

This method is similar to immunity test method of integrated circuits in the presence of conducted RF disturbances defined in IEC 62132-4. As in IEC 62132-4, the disturbance signal can be injected into I/O pins, supply pins and into the PCB reference via defined coupling networks. The EMC test board for this method can be the same as the one specified in IEC 62132-4.

The pin injection test method evaluates the performance of individual IC pins or groups of them when subjected to a transient waveform. Both positive and negative polarity transients, referenced to ground are applied. The basic test implementation is shown in Figure 1 .

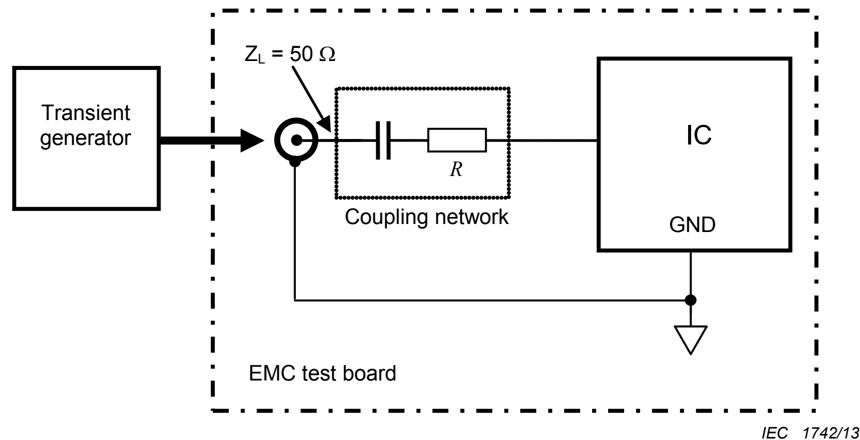

Figure 1 – Typical pin injection test implementation

5 Coupling networks

5.1 General on coupling networks

The transient disturbances are applied to the IC pin under test via defined coupling networks implemented on the PCB and connected to a device pin with respect to the pin functionality and the disturbance signal. Coupling networks are defined for:

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- supply injection;
- input injection;
- output injection;
- multiple pin injection.

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The coupling network shown in Figure 1 is identical to that used for RF immunity testing in IEC 62132-4. The series resistance (R) can be used to control the injected current, if required. The capacitance (C) is a DC block with a value selected to represent coupling effects in practice and to provide sufficient signal bandwidth while not excessively loading the connected pin (see Annex B). Default values of the series resistor and DC block capacitor are 0 Ω and 1 nF (representing capacity of 10 m parallel lines), respectively. A different capacity value may be used if required for correct functionality. The actual value of resistor and capacitor, including the rationale for their selection, shall be documented in the test report.

5.2 Supply injection network

5.2.1 Direct injection

For supply pins directly connected to the power net a direct injection as shown in Figure 2 shall be used. For these tests the coupling and decoupling networks of the transient generators standardized in IEC 61000-4-4 and IEC 61000-4-5 for industrial or ISO 7637-2 for automotive applications are used.

Mandatory blocking capacitors (C_{BL}), filter or protection components at the supply pin have to be used as recommended by the manufacturer.

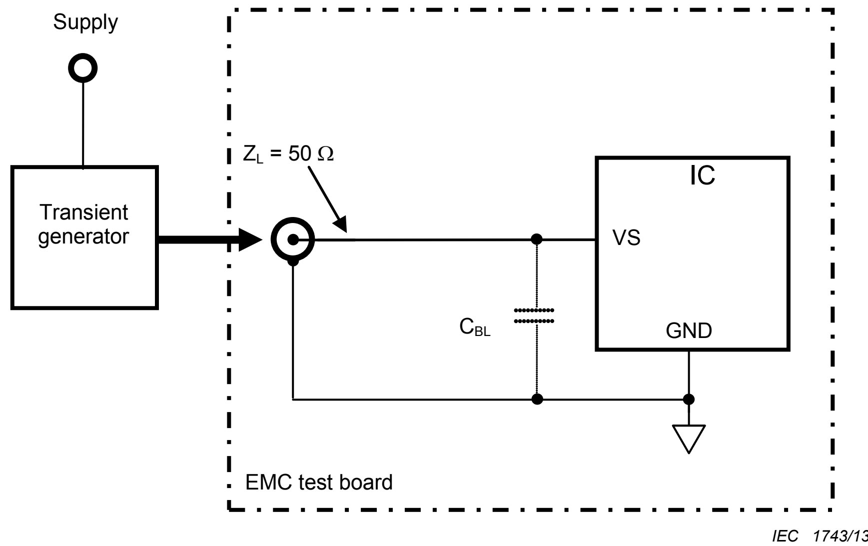

Figure 2 – Supply pin direct injection test implementation

5.2.2 Capacitive coupling

For supply pins which are not directly connected to the power net, such as global distributed sub-supply nets isolated by power converters, the test circuitry shall be implemented as shown in Figure 3. The default values of the coupling network are 0 Ω for the resistor and 1 nF for the coupling capacitor. The external DC power supply should be decoupled from the supply pin(s) of the DUT with impedance (Z) greater than 400 Ω (default) over the frequency range of the test impulse spectrum. Other values for coupling and decoupling networks are possible but must be stated in the test report (see also Clause 11).

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Mandatory blocking capacitors, filter- or protection components at the supply pin have to be used as recommended by the manufacturer.

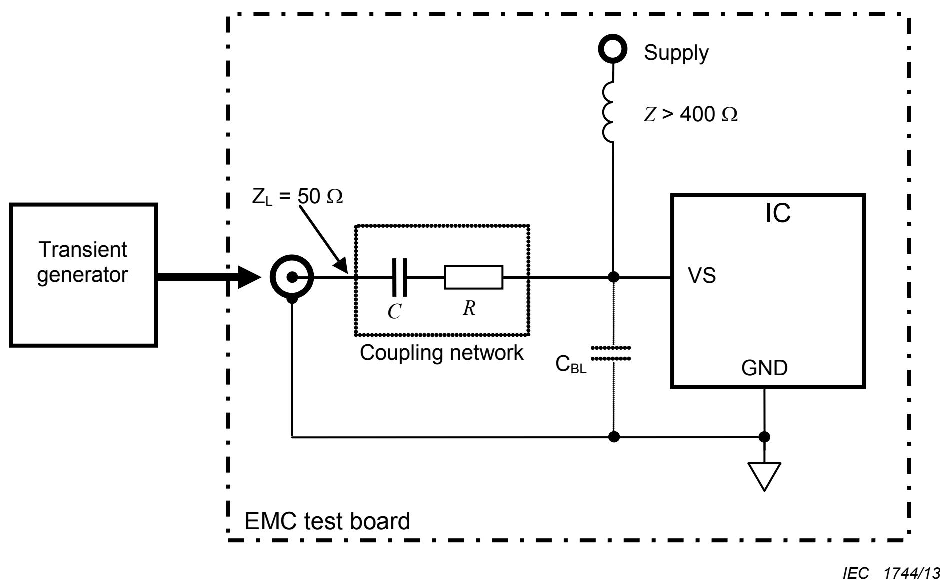

Figure 3 – Supply pin capacitive injection test implementation

5.3 Input injection

For general purpose I/O pins configured as inputs or input-only pins and globally connected, the test circuitry shall be implemented as shown in Figure 4. The default values of the

coupling network are 0 Ω for the resistor and 1 nF for the coupling capacitor. External signal sources (e.g. signal generator) which are connected to the input signal connector should be decoupled from the input pin(s) of the DUT with impedance (Z) greater than 400 Ω (default) over the frequency range of the test impulse spectrum. Other values for coupling and decoupling networks are possible but shall be stated in the test report. The input shall be configured as recommended by the manufacturer, only mandatory components have to be applied (e.g. with an appropriate external pull up resistor (R_U), a pull down resistor (R_D) or a series resistor (R_S)). The DUT function shall not be affected by the coupling network.

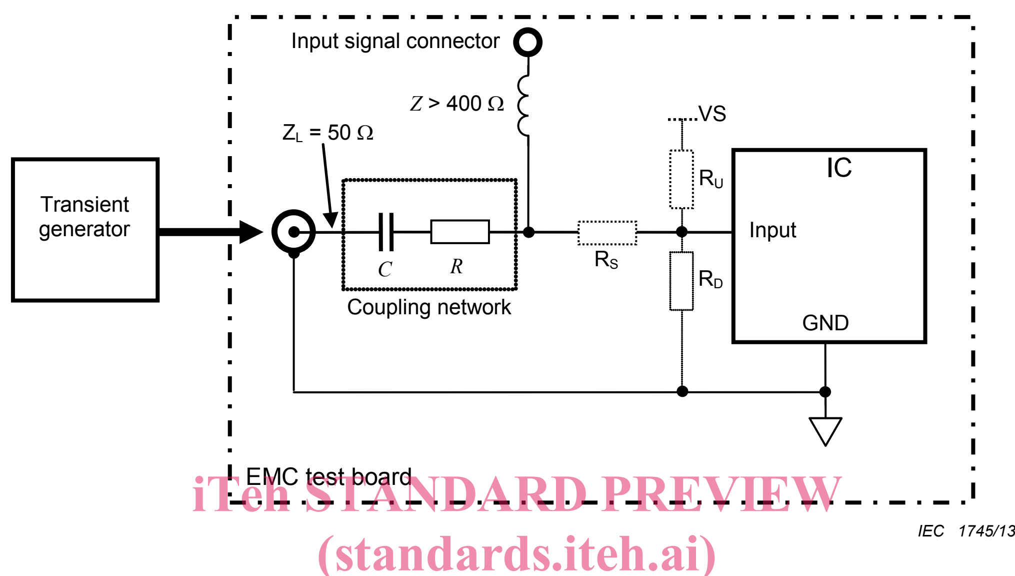

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Figure 4 – Input pin injection test implementation

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5.4 Output injection

For general purpose I/O pins configured as outputs or output-only pins and globally connected, the test circuitry shall be implemented as shown in Figure 5. The default values of the coupling network are 0 Ω for the resistor and 1 nF for the coupling capacitor. External signal processing units or loads which are connected to the output signal connector should be decoupled from the output pin(s) of the DUT with impedance (Z) greater than 400 Ω (default) over the frequency range of the test impulse spectrum. Other values can be assigned to the coupling and decoupling networks but they shall be stated in the test report. The output shall be configured and loaded (e.g. with an appropriate external capacitive load (C_L)) as specified by the manufacturer. Only mandatory external components according to the specification should be connected during test.

For output pins, the DC block capacitance shall not exceed the rated capacitive load of this output to prevent an unacceptable deviation of the output signal.

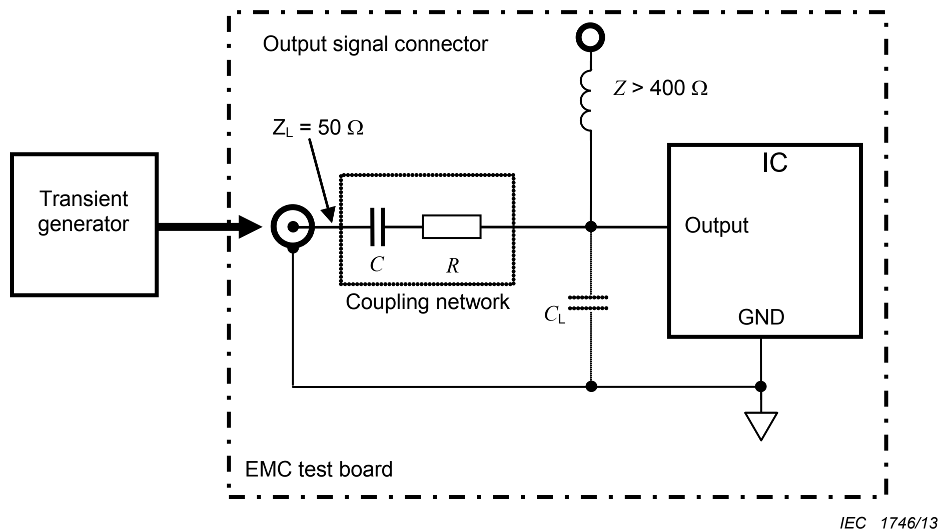

Figure 5 – Output pin injection test implementation

5.5 Simultaneous multiple pin injection

For parallel coupling to multiple pins or pin groups a coupling network consisting of one injection point and a capacitive impulse signal splitter can be used as shown in Figure 6. The default values of those coupling networks are the same as for respective single pins.

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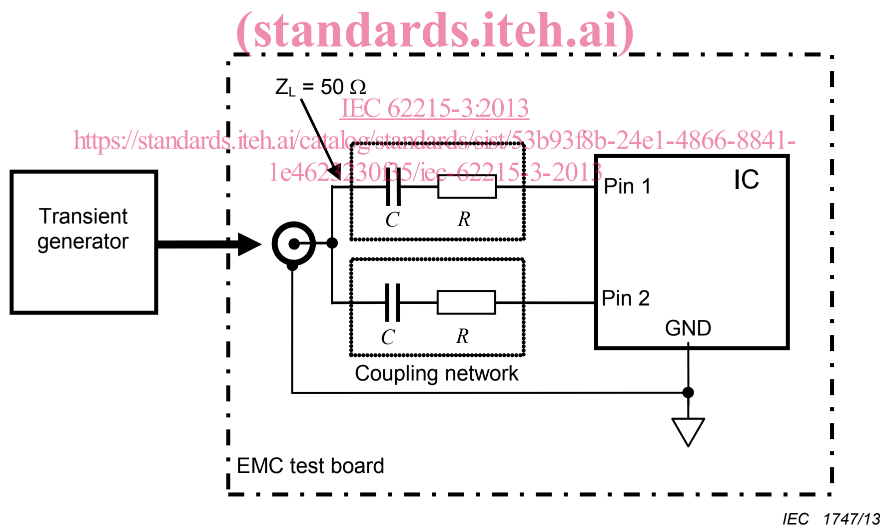

Figure 6 – Multiple pin injection test implementation

6 IC configuration and evaluation

6.1 IC configuration and operating modes

For the impulse immunity test the IC shall be set in normal operating conditions according to the typical data sheet values. This means the supply voltage shall be set to the nominal value and not to the minimum and maximum values given in the data sheet. Depending on the IC functionality relevant IC operation modes should be selected. Attempts should be made to fully exercise all functions and modes of operation that significantly influence the immunity of the DUT. If possible, the IC stimulation should be done as expected in a typical application or by auxiliary equipment not affecting the immunity performance of the DUT. When a watchdog function is available, it may be disabled during the test to collect additional information.

Mandatory components listed in the data sheet, which are necessary for the IC functionality or stimulation, shall be applied. The position of mandatory components and test board layout shall be designed not to affect adversely the test results of the IC.

NOTE To fulfil a certain test level, additional components can be necessary. Such components are regarded as mandatory for such applications.

6.2 IC monitoring

The DUT should be monitored such that immunity performance can be determined as completely as possible. The monitoring shall be implemented such that the immunity performance of the DUT is not affected.

In mixed signal ICs various response signals can be generated depending on implemented functions or installed software programs. The response signal can be monitored for indications of susceptibility that include, but are not limited to, the following parametric and functional characteristics:

- cycle-to-cycle jitter, frequency, or duty cycle of a periodic waveform;
- signal transition time (rise or fall) of the output waveform;
- signal source voltage, current or resistance;
- spikes, glitches or other transient phenomena on the output waveform;
- DUT reset;
- DUT hang;
- DUT latch-up;
- digital data loss or deviation;
- memory content corruption.

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Monitoring can be done by I/O signal detection, oscilloscopes, voltmeter, logic analyser, data analyser etc. considering certain failure criteria.

For monitored response signals, failure criteria have to be defined individually for the dedicated IC impulse immunity test. A failure criterion is defined by a nominal signal value and an allowed tolerance.

6.3 IC performance classes

The IC immunity is categorised in IC performance classes as follows:

Class A_{IC}: all monitored functions of the IC perform within the defined tolerances during and after exposure to disturbance;

Class B_{IC}: short time degradation of one or more monitored signals during exposure to disturbance is not evaluable for IC only. Therefore this classification may not be applicable for ICs (see Note);

Class C_{IC}: at least one of the monitored functions of the IC is out of the defined tolerances during the disturbance but returns automatically to the defined tolerances after the exposure to disturbance;

Class D_{IC}: at least one monitored function of the IC does not perform within the defined tolerances during exposure and does not return to normal operation by itself. The IC returns to normal operation by manual intervention;

- Class $D1_{IC}$: the IC returns to normal operation by manual intervention: (e.g. reset);
- Class $D2_{IC}$: the IC returns to normal operation by power cycling the device;

Class E_{IC}: at least one monitored function of the IC does not perform within the defined tolerances after exposure and cannot be returned to proper operation.