

INTERNATIONAL STANDARD

NORME INTERNATIONALE



**Mechanical standardization of semiconductor devices –
Part 6-12: General rules for the preparation of outline drawings of surface
mounted semiconductor device packages – Design guidelines for fine-pitch land
grid array (FLGA)**

[IEC 60191-6-12:2011](#)

<https://standards.iteh.ai/catalog/standards/sist/7c3543e4-1bc3-450e-ab26-1e4415191100>

**Normalisation mécanique des dispositifs à semiconducteurs –
Partie 6-12: Règles générales pour la préparation des dessins d'encombrement
des boîtiers des dispositifs à semiconducteurs à montage en surface – Lignes
directrices de conception pour les boîtiers matriciels à plots et à pas fins (FLGA)**



THIS PUBLICATION IS COPYRIGHT PROTECTED

Copyright © 2011 IEC, Geneva, Switzerland

All rights reserved. Unless otherwise specified, no part of this publication may be reproduced or utilized in any form or by any means, electronic or mechanical, including photocopying and microfilm, without permission in writing from either IEC or IEC's member National Committee in the country of the requester.

If you have any questions about IEC copyright or have an enquiry about obtaining additional rights to this publication, please contact the address below or your local IEC member National Committee for further information.

Droits de reproduction réservés. Sauf indication contraire, aucune partie de cette publication ne peut être reproduite ni utilisée sous quelque forme que ce soit et par aucun procédé, électronique ou mécanique, y compris la photocopie et les microfilms, sans l'accord écrit de la CEI ou du Comité national de la CEI du pays du demandeur.

Si vous avez des questions sur le copyright de la CEI ou si vous désirez obtenir des droits supplémentaires sur cette publication, utilisez les coordonnées ci-après ou contactez le Comité national de la CEI de votre pays de résidence.

IEC Central Office
3, rue de Varembe
CH-1211 Geneva 20
Switzerland
Email: inmail@iec.ch
Web: www.iec.ch

About the IEC

The International Electrotechnical Commission (IEC) is the leading global organization that prepares and publishes International Standards for all electrical, electronic and related technologies.

About IEC publications

The technical content of IEC publications is kept under constant review by the IEC. Please make sure that you have the latest edition, a corrigenda or an amendment might have been published.

- Catalogue of IEC publications: www.iec.ch/searchpub

The IEC on-line Catalogue enables you to search by a variety of criteria (reference number, text, technical committee,...). It also gives information on projects, withdrawn and replaced publications.

- IEC Just Published: www.iec.ch/online_news/justpub

Stay up to date on all new IEC publications. Just Published details twice a month all new publications released. Available on-line and also by email.

www.iec.ch/online_news/justpub

- Electropedia: www.electropedia.org

The world's leading online dictionary of electronic and electrical terms containing more than 20 000 terms and definitions in English and French, with equivalent terms in additional languages. Also known as the International Electrotechnical Vocabulary online.

- Customer Service Centre: www.iec.ch/webstore/custserv

If you wish to give us your feedback on this publication or need further assistance, please visit the Customer Service Centre FAQ or contact us:

Email: csc@iec.ch

Tel.: +41 22 919 02 11

Fax: +41 22 919 03 00

A propos de la CEI

La Commission Electrotechnique Internationale (CEI) est la première organisation mondiale qui élabore et publie des normes internationales pour tout ce qui a trait à l'électricité, à l'électronique et aux technologies apparentées.

A propos des publications CEI

Le contenu technique des publications de la CEI est constamment revu. Veuillez vous assurer que vous possédez l'édition la plus récente, un corrigendum ou amendement peut avoir été publié.

- Catalogue des publications de la CEI: www.iec.ch/searchpub/cur_fut-f.htm

Le Catalogue en-ligne de la CEI vous permet d'effectuer des recherches en utilisant différents critères (numéro de référence, texte, comité d'études,...). Il donne aussi des informations sur les projets et les publications retirées ou remplacées.

- Just Published CEI: www.iec.ch/online_news/justpub

Restez informé sur les nouvelles publications de la CEI. Just Published détaille deux fois par mois les nouvelles publications parues. Disponible en-ligne et aussi par email.

- Electropedia: www.electropedia.org

Le premier dictionnaire en ligne au monde de termes électroniques et électriques. Il contient plus de 20 000 termes et définitions en anglais et en français, ainsi que les termes équivalents dans les langues additionnelles. Egalement appelé Vocabulaire Electrotechnique International en ligne.

- Service Clients: www.iec.ch/webstore/custserv/custserv_entry-f.htm

Si vous désirez nous donner des commentaires sur cette publication ou si vous avez des questions, visitez le FAQ du Service clients ou contactez-nous:

Email: csc@iec.ch

Tél.: +41 22 919 02 11

Fax: +41 22 919 03 00

INTERNATIONAL STANDARD

NORME INTERNATIONALE



**Mechanical standardization of semiconductor devices –
Part 6-12: General rules for the preparation of outline drawings of surface
mounted semiconductor device packages – Design guidelines for fine-pitch land
grid array (FLGA)**

[IEC 60191-6-12:2011](https://standards.iteh.ai/catalog/standards/sist/7c3543e4-1bc3-450e-ab26-4e44c368c111/iec-60191-6-12-2011)

<https://standards.iteh.ai/catalog/standards/sist/7c3543e4-1bc3-450e-ab26-4e44c368c111/iec-60191-6-12-2011>

**Normalisation mécanique des dispositifs à semiconducteurs –
Partie 6-12: Règles générales pour la préparation des dessins d'encombrement
des boîtiers des dispositifs à semiconducteurs à montage en surface – Lignes
directrices de conception pour les boîtiers matriciels à plots et à pas fins (FLGA)**

INTERNATIONAL
ELECTROTECHNICAL
COMMISSION

COMMISSION
ELECTROTECHNIQUE
INTERNATIONALE

PRICE CODE
CODE PRIX

R

ICS 31.080.01

ISBN 978-2-88912-527-2

CONTENTS

FOREWORD.....	3
1 Scope.....	5
2 Normative references	5
3 Terms and definitions	5
4 Terminal position numbering.....	6
5 Nominal package dimension	6
6 Outline drawings and principle dimensions	7
7 Dimensions	10
Figure 1 – Flange-type FLGA.....	6
Figure 2 – Rectangle-type FLGA.....	6
Figure 3 – Flange-type FLGA.....	7
Figure 4 – Rectangle-type FLGA.....	8
Figure 5 – Mechanical gauge drawing ^e	9
Figure 6 – Pattern of terminal position area ^f	9
Table 1 – Group 1: Dimensions appropriate to mounting and interchangeability.....	10
Table 2 – Group 2: Dimensions and tolerances.....	14
Table 3 – Combination list of D, E, M _D , and M _E – $\square = 0,80$ mm pitch.....	15
Table 4 – Combination list of D, E, M _D , and M _E – $\square = 0,65$ mm pitch	16
Table 5 – Combination list of D, E, M _D , and M _E – $\square = 0,50$ mm pitch	17
Table 6 – Combination list of D, E, M _D , and M _E – $\square = 0,40$ mm pitch	18
Table 7 – Combination list of D, E, M _D , and M _E – $\square = 0,30$ mm pitch	19

INTERNATIONAL ELECTROTECHNICAL COMMISSION

MECHANICAL STANDARDIZATION OF SEMICONDUCTOR DEVICES –**Part 6-12: General rules for the preparation of outline drawings
of surface mounted semiconductor device packages –
Design guidelines for fine-pitch land grid array (FLGA)**

FOREWORD

- 1) The International Electrotechnical Commission (IEC) is a worldwide organization for standardization comprising all national electrotechnical committees (IEC National Committees). The object of IEC is to promote international co-operation on all questions concerning standardization in the electrical and electronic fields. To this end and in addition to other activities, IEC publishes International Standards, Technical Specifications, Technical Reports, Publicly Available Specifications (PAS) and Guides (hereafter referred to as “IEC Publication(s)”). Their preparation is entrusted to technical committees; any IEC National Committee interested in the subject dealt with may participate in this preparatory work. International, governmental and non-governmental organizations liaising with the IEC also participate in this preparation. IEC collaborates closely with the International Organization for Standardization (ISO) in accordance with conditions determined by agreement between the two organizations.
- 2) The formal decisions or agreements of IEC on technical matters express, as nearly as possible, an international consensus of opinion on the relevant subjects since each technical committee has representation from all interested IEC National Committees.
- 3) IEC Publications have the form of recommendations for international use and are accepted by IEC National Committees in that sense. While all reasonable efforts are made to ensure that the technical content of IEC Publications is accurate, IEC cannot be held responsible for the way in which they are used or for any misinterpretation by any end user.
- 4) In order to promote international uniformity, IEC National Committees undertake to apply IEC Publications transparently to the maximum extent possible in their national and regional publications. Any divergence between any IEC Publication and the corresponding national or regional publication shall be clearly indicated in the latter.
- 5) IEC itself does not provide any attestation of conformity. Independent certification bodies provide conformity assessment services and, in some areas, access to IEC marks of conformity. IEC is not responsible for any services carried out by independent certification bodies.
- 6) All users should ensure that they have the latest edition of this publication.
- 7) No liability shall attach to IEC or its directors, employees, servants or agents including individual experts and members of its technical committees and IEC National Committees for any personal injury, property damage or other damage of any nature whatsoever, whether direct or indirect, or for costs (including legal fees) and expenses arising out of the publication, use of, or reliance upon, this IEC Publication or any other IEC Publications.
- 8) Attention is drawn to the Normative references cited in this publication. Use of the referenced publications is indispensable for the correct application of this publication.
- 9) Attention is drawn to the possibility that some of the elements of this IEC Publication may be the subject of patent rights. IEC shall not be held responsible for identifying any or all such patent rights.

International Standard IEC 60191-6-12 has been prepared by subcommittee 47D: Mechanical standardization of semiconductor devices, of IEC technical committee 47: Semiconductor devices.

This second edition of IEC 60191-6-12 cancels and replaces the first edition, published in 2002 and constitutes a technical revision. This edition includes the following significant changes with respect to the previous edition:

- a) scope is expanded so that this standard include the square type FLGA. The title of this standard has been changed accordingly: “Rectangular type” has been deleted from the title.
- b) ball pitch of 0,3 mm has been added;
- c) datum is changed from the body datum to the ball datum;
- d) combination lists of D , E , M_D , and M_E have been revised.

The text of this standard is based on the following documents:

CDV	Report on voting
47D/784/CDV	47D/795/RVC

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

A list of all the parts in the IEC 60191 series, under the general title *Mechanical standardization of semiconductor devices*, can be found on the IEC website.

The committee has decided that the contents of this publication will remain unchanged until the stability date indicated on the IEC web site under "<http://webstore.iec.ch>" in the data related to the specific publication. At this date, the publication will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

iTeh STANDARD PREVIEW

IMPORTANT – The 'colour inside' logo on the cover page of this publication indicates that it contains colours which are considered to be useful for the correct understanding of its contents. Users should therefore print this document using a colour printer.

<https://standards.iteh.ai/catalog/standards/sist/7c3543e4-1bc3-450e-ab26-e3dc4c301380/iec-60191-6-12-2011>

MECHANICAL STANDARDIZATION OF SEMICONDUCTOR DEVICES –

Part 6-12: General rules for the preparation of outline drawings of surface mounted semiconductor device packages – Design guidelines for fine-pitch land grid array (FLGA)

1 Scope

This part of IEC 60191 provides standard outline drawings, dimensions, and recommended variations for all fine-pitch land grid array packages (FLGA) with terminal pitch of 0,8 mm or less.

2 Normative references

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60191(all parts), *Mechanical standardization of semiconductor devices*

IEC 60191-6, *Mechanical standardization of semiconductor devices – Part 6: General rules for the preparation of outline drawings of surface mounted semiconductor device packages*

3 Terms and definitions

[IEC 60191-6-12:2011](https://standards.iteh.ai/catalog/standards/sist/7c3543e4-1bc3-450e-ab26-e3dc4c301380/iec-60191-6-12-2011)

<https://standards.iteh.ai/catalog/standards/sist/7c3543e4-1bc3-450e-ab26-e3dc4c301380/iec-60191-6-12-2011>

For the purposes of this document, the terms and definitions given IEC 60191 series and the following apply.

3.1

fine-pitch land grid array

FLGA

package with metal lands on one side of a substrate in a matrix of at least three rows and three columns on a pitch of 0,8 mm or less, wherein the maximum standoff height is 0,10 mm or less

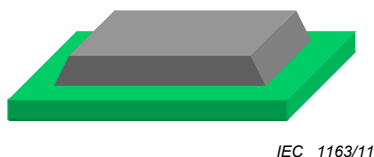
NOTE Terminals may be missing from some row-column intersections.

3.2

flange-type FLGA

FLGA with a package outline (length, width) defined by a package flange part, mostly substrate, extending outward beyond the perimeter of a molded part or of a flip-chip-bonded part

NOTE Flange-type FLGA, shown in Figure 1, is generally cut by singulation press, thus resulting in larger dimensional errors than the singulation by dicing saw



IEC 1163/11

Figure 1 – Flange-type FLGA

**3.3
rectangle-type FLGA**

FLGA with a package outline (length, width) defined by a molded part with no extending flange part

NOTE Rectangle-type FLGA, shown in Figure 2, is generally cut by dicing, thus resulting in less dimensional errors than the singulation by press machine.



Figure 2 – Rectangle-type FLGA

4 Terminal position numbering [IEC 60191-6-12:2011](https://standards.iteh.ai/catalog/standards/sist/7c3543e4-1bc3-450e-ab26-e3dc4c301380/iec-60191-6-12-2011)

When a package is viewed from the terminal side with the index corner in the bottom left corner position, terminal rows are lettered from bottom to top starting with A, then B, C,,, AA, AB, etc., whereas terminal columns are numbered from left to right starting with 1. Terminal positions are designated by a row-column grid system and shown as alphanumeric identification, e.g., A1, B1.

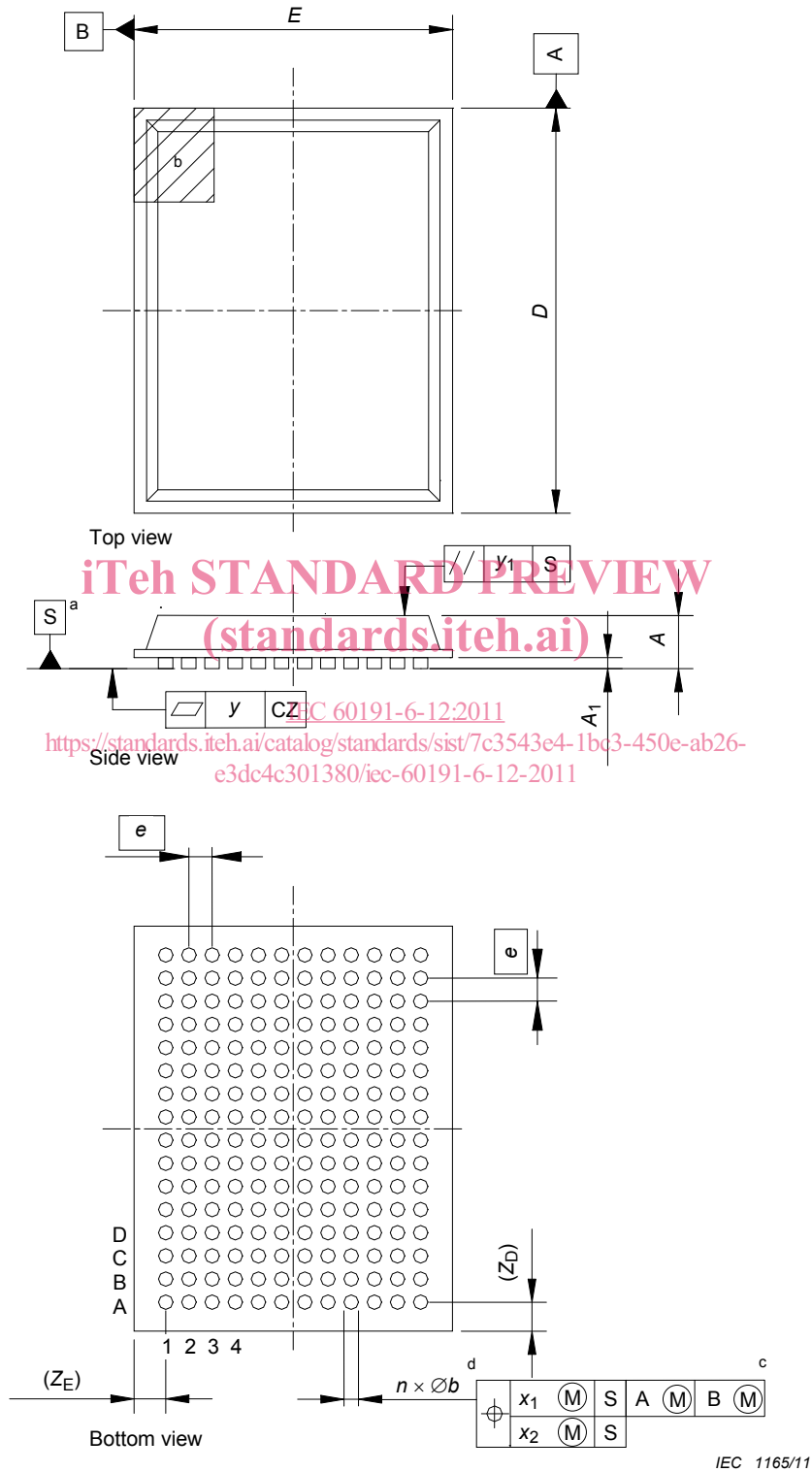
The letters I, O, Q, S, X and Z shall not be used for naming the terminal rows.

5 Nominal package dimension

A nominal package dimension is defined as “the package width (*E*) × length (*D*)”, which is expressed in the tenths place in millimeter.

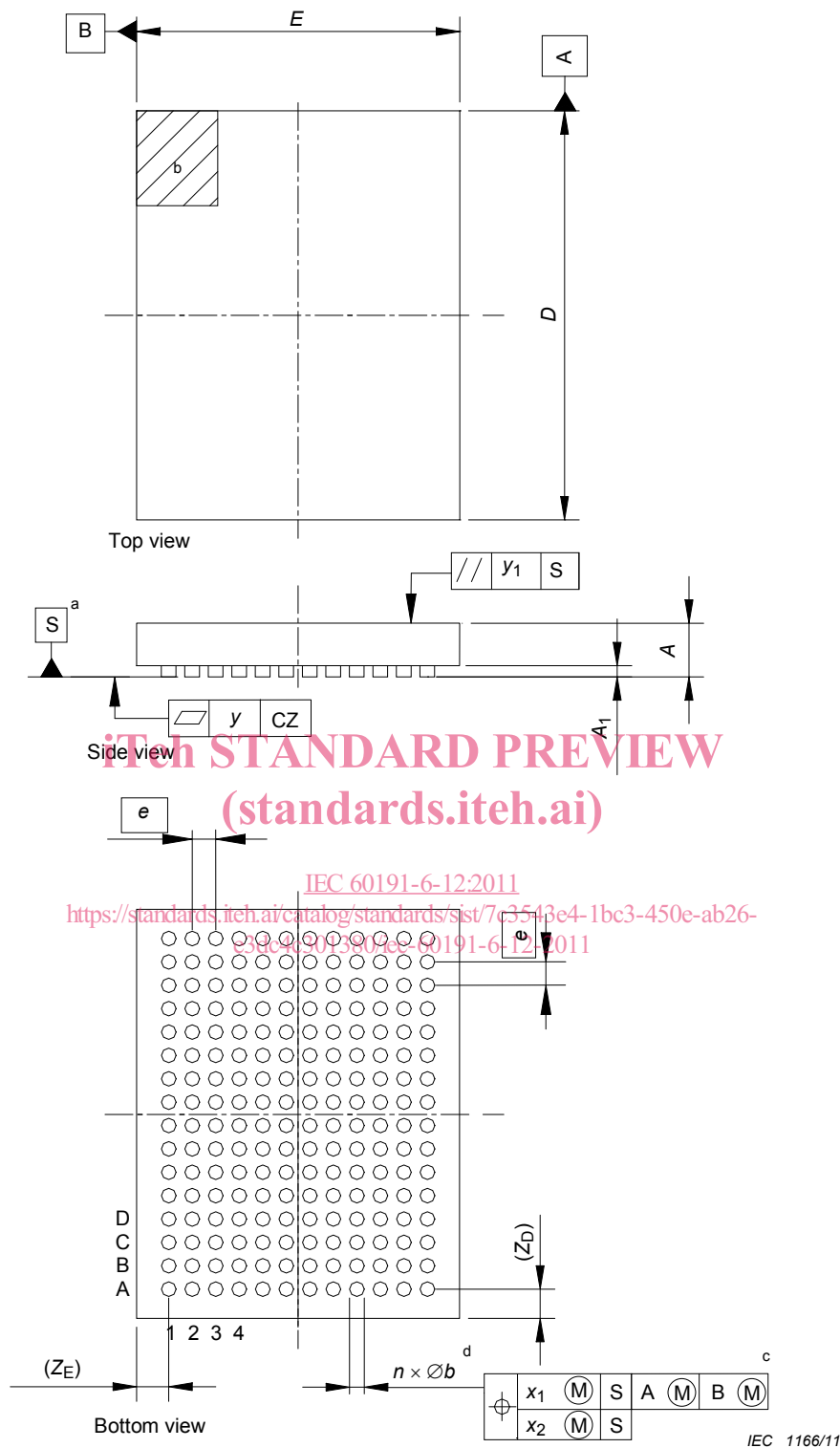
6 Outline drawings and principle dimensions

The FLGA outline is shown in Figures 3 and 4.



NOTE For footnotes relating to this figure, see Figure 4.

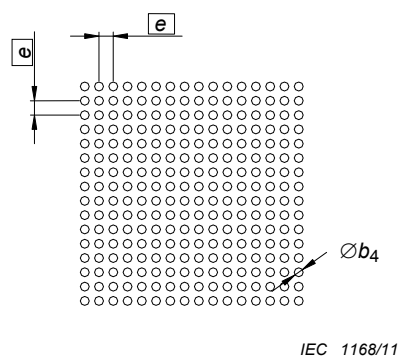
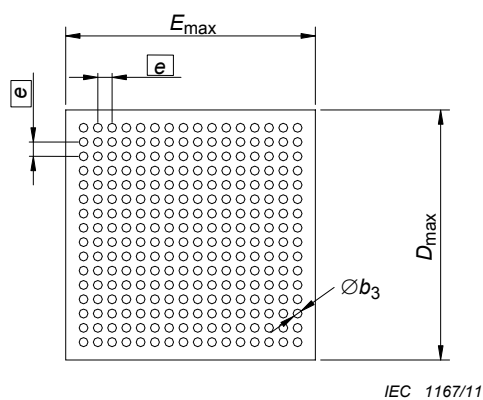
Figure 3 – Flange-type FLGA



NOTES relating to Figures 3 and 4:

- ^a Datum S is defined as the seating plane on which a package free stands by contact of the balls.
- ^b The hatched zone is an index-marking area, where whole index mark will be basically contained in 1/16 of the body size. In case it is physically difficult, index mark can extend more than 1/16 but no more than a quarter of the body size.
- ^c True positional tolerances of terminals, x_1 and x_2 , are applied to all terminals.
- ^d The terminal diameter b is the maximum diameter of individual balls as measured in the plane parallel to the seating plane.
- ^e An array of terminal-existence areas with regard to the datum S , A , and B is shown in the mechanical gauge drawing in Figure 5.
- ^f The array of terminal-existence areas with regard to the datum S is shown in Figure 6.

Figure 4 – Rectangle-type FLGA



NOTE The symbols in this figure are explained in IEC 60191-6.

Figure 5 – Mechanical gauge drawing ^e

Figure 6 – Pattern of terminal position area ^f

iTeh STANDARD PREVIEW (standards.iteh.ai)

[IEC 60191-6-12:2011](https://standards.iteh.ai/catalog/standards/sist/7c3543e4-1bc3-450e-ab26-e3dc4c301380/iec-60191-6-12-2011)

<https://standards.iteh.ai/catalog/standards/sist/7c3543e4-1bc3-450e-ab26-e3dc4c301380/iec-60191-6-12-2011>

7 Dimensions

Table 1 – Group 1: Dimensions appropriate to mounting and interchangeability

Dimensions in millimeters

Term	Symbol	Specification	Recommended value
Package nominal dimension	$E \times D$	A package nominal dimension is defined as "the package width (E) x length (D), which is expressed in the tenths place in millimeter.	-
Package length	D	<p>(1) Range of D_{nom}: from 1,5 to 21,0</p> <p>(2) Interval of D_{nom} For square FLGA with $D_{nom} \geq 15,0$, D_{nom} is an integer. For other FLGA, the number in the tenths place of D_{nom} is either 0 or 5.</p> <p>(3) Tolerance of D For Flange-type: When $D_{nom} \leq 21,0$, $v_D = \pm 0,15$ When $D_{nom} > 21,0$, $v_D = \pm 0,20$ where v_D denotes a tolerance.</p> <p>For Rectangle-type: When $D_{nom} \leq 12,0$, $v_D = \pm 0,08$ When $12,0 < D_{nom} \leq 21,0$, $v_D = \pm 0,10$ When $D_{nom} > 21,0$, $v_D = \pm 0,15$ where v_D denotes a tolerance.</p>	-

Table 1 (continued)

Dimensions in millimeters

Term	Symbol	Specification	Recommended value
Package width	E	<p>(1) Range of E_{nom}: from 1,5 to 21,0</p> <p>(2) Interval of E_{nom} For square FLGA with $E_{nom} \geq 15,0$, E_{nom} is an integer. For other FLGA, the number in the tenths place of E_{nom} is either 0 or 5.</p> <p>(3) Tolerance of "E" For flange-type: When $E_{nom} \leq 21,0$, $v_E = \pm 0,15$ When $E_{nom} > 21,0$, $v_E = \pm 0,20$ where v_E denotes a tolerance.</p> <p>For rectangle-type: When $E_{nom} \leq 12,0$, $v_E = \pm 0,08$ When $12,0 < E_{nom} \leq 21,0$, $v_E = \pm 0,10$ When $E_{nom} > 21,0$, $v_E = \pm 0,15$ where v_E denotes a tolerance.</p>	-
Maximum profile height	A	<p>$A = 0,30$ 0,40 0,50 0,65 0,80 1,00 1,20 1,70 2,00</p> <p>"A" includes heat slug thickness, package warpage, and tilt errors.</p>	-
Stand-off height	A_1	$A_1 \max \leq 0,10$	-
Terminal grid pitch	e	<p>$e = 0,80$ 0,65 0,50 0,40 0,30</p>	-