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Standard Test Methods for Edge Contour of Circular Semiconductor Wafers and Rigid Disk Substrates[1]

This standard is issued under the fixed designation F 928; the number immediately following the designation indicates the year of original adoption or, in the case of revision, the year of last revision. A number in parentheses indicates the year of last reapproval. A superscript epsilon (ϵ) indicates an editorial change since the last revision or reapproval.

1. Scope

1.1 These test methods[2] provide means for examining the edge contour of circular wafers of silicon, gallium arsenide, and other electronic materials, and determining fit to limits of contour specified by a template that defines a permitted zone through which the contour must pass. Principal application of such a template is intended for, but not limited to, wafers that have been deliberately edge shaped.

1.2 Two test methods are described. One is destructive and is limited to inspection of discrete points on the periphery, including flats. The contour of deliberately edge-shaped wafers may not be uniform around the entire periphery, and thus the discrete location(s) may or may not be representative of the entire periphery. The other test method is nondestructive and suitable for inspection of all points on the wafers periphery except flats.

1.3 The nondestructive test method may also be applied to the examination of the edge contour of the outer periphery of substrates for rigid disks used for magnetic storage of data.

NOTE 1—Reference to wafers in the remainder of this standard shall be interpreted to include substrates for rigid disks unless the phrase "of electronic materials" is also included in the context.

1.4 The values stated in SI units are to be regarded as the standard. The values given in parentheses are for information only.

1.5 *This standard does not purport to address all of the safety concerns, if any, associated with its use. It is the responsibility of the user of this standard to establish appropriate safety and health practices and determine the applicability of regulatory limitations prior to use.*

2. Referenced Documents

2.1 *ASTM Standards:*

E 122 Practice for Choice of Sample Size to Estimate a Measure of Quality for a Lot or Process[3]

2.2 *Military Standard:*

MIL-STD-105D Sampling Procedures and Tables for Inspection by Attributes[4]

2.3 *SEMI Standards:*

SEMI M1, Specifications for Polished Monocrystalline Silicon Wafers[5]

SEMI M9, Specifications for Polished Monocrystalline Gallium Arsenide Slices[5]

3. Summary of Test Methods

3.1 Both test methods employ optical means to project a shadow of the edge contour at substantial magnification on a screen. In applying Method A (destructive) the sample wafer is cleaved or broken along a diameter. A sharply focused image of the cross section of the wafer is obtained over a sufficiently large region near the edge with the aid of an optical comparator or projection microscope. In Method B (nondestructive) the unbroken wafer is back lighted with collimated (parallel) light such that a sharply defined shadow of the wafer edge is projected on a screen. In this test method the wafer is not altered in any way.

3.2 By either test method, the contour of the wafer edge profile image is compared to a template that has been mounted or projected on the screen. The template defines a permitted zone through which the edge contour must pass.

4. Significance and Use

4.1 The edges of circular wafers of electronic materials are frequently required to be shaped after cutting the wafers from the ingot. Contouring the wafer edge reduces the incidence of chipping and minimizes epitaxial edge crown and photoresist edge bead during subsequent processing of the wafer. Similarly, edges of rigid disk substrates are frequently edge shaped.

4.2 The test methods described here provide means to determine that the wafer edge contour is appropriate to meet specifications, such as SEMI M1 or SEMI M9, which are intended to provide wafers avoiding the difficulties enumerated above.

[1] These test methods are under the jurisdiction of ASTM Committee F-1 on Electronics and are the direct responsibility of Subcommittee F01.06 on Silicon Materials and Process Control.

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[2] DIN 50441/2 is equivalent to Method B of this standard. It is the responsibility of DIN Committee NMP 221 with which Committee F-1 maintains close technical liaison. DIN 50441/2, Measurement of the Geometric Dimensions of Semiconductor Slices; Testing of Edge Rounding, is available from Beuth Verlag GmbH, Burggrafenstrasse 4-10, D-1000 Berlin 30, FRG.

[3] *Annual Book of ASTM Standards*, Vol 14.02.

[4] Available from Standardization Documents Order Desk, Bldg. 4 Section D, 700 Robbins Ave., Philadelphia, PA 19111-5094, Attn: NPODS.

[5] Available from the Semiconductor Equipment and Materials International, 805 East Middlefield Road, Mountain View, CA 94043.

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4.3 Method A is recommended for examining the edge profile of flatted regions of the wafer.

4.4 Method A is best suited for referee purposes. Method B is appropriate for routine process monitoring such as alignment of wafer edge grinders, routine quality control and incoming/outgoing inspection purposes. In view of the uncertainty of precisely locating the intersection of the contour and the wafer surface when carrying out Method B, use of this method for commercial transactions is not recommended unless the parties to the test establish the degree of correlation that can be obtained.

4.5 Method B is suitable for examining the outer circumference or rigid disk substrates; metallic rigid disk substrates cannot conveniently be cleaved.

5. Interferences

5.1 In Method B, the profile of the parallel surfaces of the wafer may not be sharply focused at distances exceeding approximately 0.5 mm (0.020 in.) from the extreme wafer edge toward the wafer center. This uncertainty in the wafer surface location may cause inaccuracy in positioning the wafer with respect to template lines. It may also make it difficult to determine whether the wafer edge profile lies within the permitted zone at point B of the template. These difficulties can be overcome by aligning a straight edge to the wafer surface by direct contact, observing the shadow extension in the sharply focused region, and extrapolating the straight line edge of the template reference. In applying this technique, exercise care to avoid damaging or contaminating the wafer surface.

5.1.1 This limitation renders Method B unsuitable for determining the distance between the front and back wafer surfaces. The edge contours near the front and back surfaces of the wafer must be inspected separately.

5.2 In Method B, attempting to view the complete wafer periphery, except flats, through wafer rotation necessitates frequent focus adjustment due to variations in wafer roundness and fixturing precision, including wafer centering.

5.3 By either test method, any foreign material such as large particles or high spots on the wafer surface in the light path will present a false edge contour by masking the true contour shape.

5.4 It is not always feasible to provide a uniform radius or bevel to the edges of wafers because silicon, gallium arsenide, and many other electronic materials as well as glass disk substrates are both hard and brittle. Wear of grinding tools, process variations, and the presence of flats on the circumference of wafers cause practical contours to have varying shapes. For this reason, templates are used that define an allowed range.

5.5 If a television system is used, the user is cautioned that distortions in the horizontal and vertical deflections may occur. (See 9.2.)

6. Apparatus

6.1 For Method A, an optical comparator or projection microscope capable of 100× magnification with viewing screen large enough to permit display of an area 1 by 1 mm (0.04 by 0.04 in.).

6.2 For Method B, a collimated light source (coherent or incoherent) and a television system, consisting of a camera, lenses to give 100× magnification and TV monitor capable of displaying a 1 by 1-mm (0.04 by 0.04-in.) area.

NOTE 2—An adjustable camera mount, slice holding fixture, or lens adjustment is desirable for sharp focusing.

6.3 *Fixture*, for holding the wafer to be tested. The fixture must provide means for positioning the wafer such that the plane of the surface of the wafer is parallel to the viewing direction. The fixture should be arranged in such a way that its position and orientation in a plan perpendicular to the viewing direction can be adjusted conveniently, or alternatively, the template can be moved. Optionally, for Method B, the fixture can provide means for rotation of the wafer about its axis of symmetry. The design of the fixture for Method B should be such that the wafer may be loaded, held in position, and unloaded with minimum risk of contamination or damage to the wafer.

6.4 *Template*, having transparent regions defining the area through which the contour of the edge of the wafer must pass and a semi-transparent region bounding the space. An example of a template is given in Fig. 1. Instructions for constructing templates are given in Section 10.

6.5 *Gage Block or Precision Rod*, with dimensions approximately the same as the thickness of the wafer to be tested and accurately known for use in establishing the magnification of the apparatus.

6.6 *Rule*, 150 mm (6 in.) long with scale gradations of 0.5 mm (0.02 in.) or less.

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7. Sampling

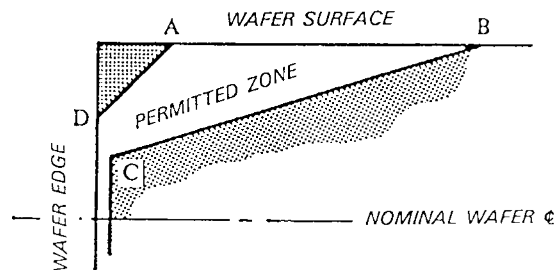
7.1 Unless otherwise specified, Practice E 122 shall be used. When so specified, appropriate sample sizes shall be selected from each lot in accordance with MIL-STD-105D. Inspection levels shall be agreed upon between the supplier and purchaser.

7.2 The number and location of the test points on the periphery of each wafer shall be agreed upon between the supplier and purchaser.

8. Specimen Preparation

8.1 For Method A, cleave or fracture the wafer along a diameter.

NOTE 3—This may be conveniently accomplished by positioning the wafer over a small diameter rod and pressing downward on both sides. (Alignment by eye is sufficient.) If required by the sampling plan, cleave additional pieces along the edge of the wafer.



NOTE 1—Only half is used to emphasize that these methods are not intended for measurement of thickness.

FIG. 1 Template Showing One Half of Water Cross Section