Designation: F 1152 – 93 (Reapproved 2001)

Standard Test Method for Dimensions of Notches on Silicon Wafers[1]

This standard is issued under the fixed designation F 1152; the number immediately following the designation indicates the year of original adoption or, in the case of revision, the year of last revision. A number in parentheses indicates the year of last reapproval. A superscript epsilon (ε) indicates an editorial change since the last revision or reapproval.

1. Scope

1.1 This test method covers a nondestructive procedure to determine whether or not the dimensions of fiducial notches on silicon wafers fall within specified limits.

1.2 The values stated in SI units are to be regarded as the standard. The values given in parentheses are for information only.

1.3 *This standard does not purport to address all of the safety concerns, if any, associated with its use. It is the responsibility of the user of this standard to establish appropriate safety and health practices and determine the applicability of regulatory limitations prior to use.*

2. Referenced Documents

2.1 *ASTM Standards:*

E 122 Practice for Choice of Sample Size to Estimate a Measure of Quality of a Lot or Process [2]

2.2 *Military Standard:*

MIL-STD-105E Sampling Procedures and Tables for Inspection by Attributes [3]

2.3 *SEMI Standard:*

M 1 Specifications for Monocrystalline Silicon Wafers [4]

3. Summary of Test Method

3.1 The wafer is aligned in position on an optical comparator and the image of the notch is compared with a series of templates projected on the screen of the comparator.

3.2 First, the wafer is aligned so that the sides of the image of the notch contact the image of the alignment pin used to fix the position of the wafer in use. In this case, the image of the notch bottom must lie on or below the designated line on the notch form/depth template and the image of the wafer edge must lie on or above another designated line on the template.

3.3 The wafer is then aligned so that the image of the wafer edge coincides with the wafer periphery line on the template. In this case the image of the notch bottom must lie between maximum and minimum lines on the template.

3.4 The image of the notch sides are compared with a series of angles on the notch angle template and the angle that makes the best fit is chosen as the value of the notch angle.

3.5 No test is provided for the blend radius at the apex of the notch.

4. Significance and Use

4.1 Wafers must be accurately aligned in various processing equipment during integrated circuit manufacture.

4.2 A notch ground into the edge of the wafer at a specified orientation provides a positive method for such alignment. The accuracy of the critical dimensions of the notch controls the possible accuracy of the alignment.

4.3 This test method is specifically directed to the notch dimensions specified in SEMI Specifications M 1, but with suitable modifications, the principles of this test method may be applied to any desired notch dimensions.

4.4 This test method may be used for process control, quality control, and incoming or outgoing inspection.

4.5 Until an index of precision is determined based on an interlaboratory evaluation, this test method is not recommended for use in decisions between purchasers and suppliers.

5. Interferences

5.1 Any foreign material or rough spots on the notch edge in the light path may present a distorted image which can result in the determination of incorrect dimensions.

5.2 Alignment of the notch position with respect to the center of the wafer is important in achieving an accurate determination of the notch characteristics.

5.3 Wear of grinding tools and process variations may result in notch edges which are not exactly straight and a nonunique radius at the apex of the notch. Under these conditions, great care must be taken to align the image of the notch correctly against the appropriate portions of the template.

6. Apparatus

6.1 *Optical Comparator*, capable of 20 and 50× magnification with a viewing screen large enough to display an area 5 by 5 mm at 20× or 2 by 2 mm at 50×.

6.2 *Fixture*, for holding the wafer to be tested. The fixture must provide means for positioning the wafer such that the plane of the surface of the wafer is perpendicular to the viewing direction and that the wafer can be rotated about its center. The horizontal and vertical motions are parallel or

[1] This test method is under the jurisdiction of ASTM Committee F01 on Electronics and is the direct responsibility of Subcommittee F01.06 on Silicon Materials and Process Control.

Current edition approved Aug. 15, 1993. Published October 1993. Originally published as F 1152 – 88. Last previous edition F 1152 – 88.

[2] *Annual Book of ASTM Standards*, Vol 14.02.

[3] Available from Standardization Documents Order Desk, Bldg. 4 Section D, 700 Robbins Ave., Philadelphia, PA 19111-5094, Attn: NPODS.

[4] Available from the Semiconductor Equipment and Materials Institute, 805 Middlefield Rd., Mountain View, CA 94043.