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Designation: F 534 – 97

AMERICAN SOCIETY FOR TESTING AND MATERIALS
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Standard Test Method for Bow of Silicon Wafers[1]

This standard is issued under the fixed designation F 534; the number immediately following the designation indicates the year of original adoption or, in the case of revision, the year of last revision. A number in parentheses indicates the year of last reapproval. A superscript epsilon (ε) indicates an editorial change since the last revision or reapproval.

1. Scope

1.1 This test method covers determination of the average amount of bow of nominally circular silicon wafers, polished or unpolished, in the free (non-clamped) condition.

1.2 This test method is intended primarily for use with wafers that meet the dimension and tolerance requirements of SEMI Specifications M1.

1.3 This test method can also be applied to circular wafers of other semiconducting materials, such as gallium arsenide, or electronic substrate materials, such as sapphire or gadolinium gallium garnet, that have a diameter of 25 mm or greater, a thickness of 0.18 mm or greater, and a ratio of diameter to thickness up to 250. Wafers to be tested may have one or more fiducial flats provided they are located in such a way that the slice can be centered on the support pedestals (see 7.1.2) without falling off.

1.4 The values stated in inch-pound units are to be regarded as the standard. The values given in parentheses are for information only.

1.5 *This standard does not purport to address the safety concerns, if any, associated with its use. It is the responsibility of the user of this standard to establish appropriate safety and health practices and determine the applicability of regulatory limitations prior to use.*

2. Referenced Documents

2.1 *ASTM Standards:*

F 533 Test Method for Thickness and Thickness Variation of Silicon Slices[2]

F 657 Test Method for Measuring Warp and Total Thickness Variation on Silicon Wafers by Noncontact Scanning[2]

2.2 *SEMI Standard:*

M1 Specifications for Polished Monocrystalline Silicon Slices[3]

2.3 *Federal Standard:*

Fed. Std. No. 209B Controlled Environment Clean Room and Work Station Requirements[4]

3. Terminology

3.1 *Definitions:*

3.1.1 *back surface—of a semiconductor wafer,* the exposed surface opposite to that upon which active semiconductor devices have been or will be fabricated.

3.1.2 *bow—of a semiconductor wafer,* the deviation of the center point of the median surface of a free, unclamped wafer from a median-surface reference plane established by three points equally spaced on a circle with diameter a specified amount less than the nominal diameter of the wafer.

3.1.2.1 *Discussion*—If the median surface of a free, unclamped wafer has a curvature that is everythere the same, bow is a measure of its concave or convex deformation, independent of any thickness variation that may be present. Positive values of bow denote a convex (mounded) median surface when the wafer is positioned with its front surface up. Conversely, negative values of bow denote a concave (dished) median surface when the wafer is positioned with its front surface up. Although bow may be caused by unequal stresses on the two exposed surfaces of the wafer, it cannot be determined from measurements on a single exposed surface.

3.1.3 *front surface—of a semiconductor wafer,* the exposed surface upon which active semiconductor devices have been or will be fabricated.

3.1.4 *median surface—of a semiconductor wafer,* the locus of points in the wafer equidistant between the front and back surfaces.

4. Summary of Test Method

4.1 The wafer is supported, front surface upward, on three points equally spaced on the circumference of a circle whose diameter is slightly smaller than the wafer diameter. The distance between the center point of the front surface and the reference plane formed by the three supporting points is measured with a lightly loaded indicator. The wafer is turned over and the measurement is repeated with the wafer supported at three points directly opposite (through the thickness of the wafer) from the original three points. An average value of the bow of the wafer is calculated from these two measurements.

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[1] This test method is under the jurisdiction of ASTM Committee F-1 on Electronics and is the direct responsibility of Subcommittee F01.06 on Silicon Materials and Process Control.

Current edition approved June 10, 1997. Published August 1997. Originally published as F534 – 77 T. Last previous edition F534 – 91.

[2] *Annual Book of ASTM Standards*, Vol 10.05.

[3] Available from Semiconductor Equipment and Materials International, 805 E. Middlefield Rd., Mountain View, CA 94043.

[4] Available from GSA Business Service Centers in Boston, New York, Atlanta, Chicago, Kansas City, MO, Fort Worth, Denver, Seattle, San Francisco, and Los Angeles.