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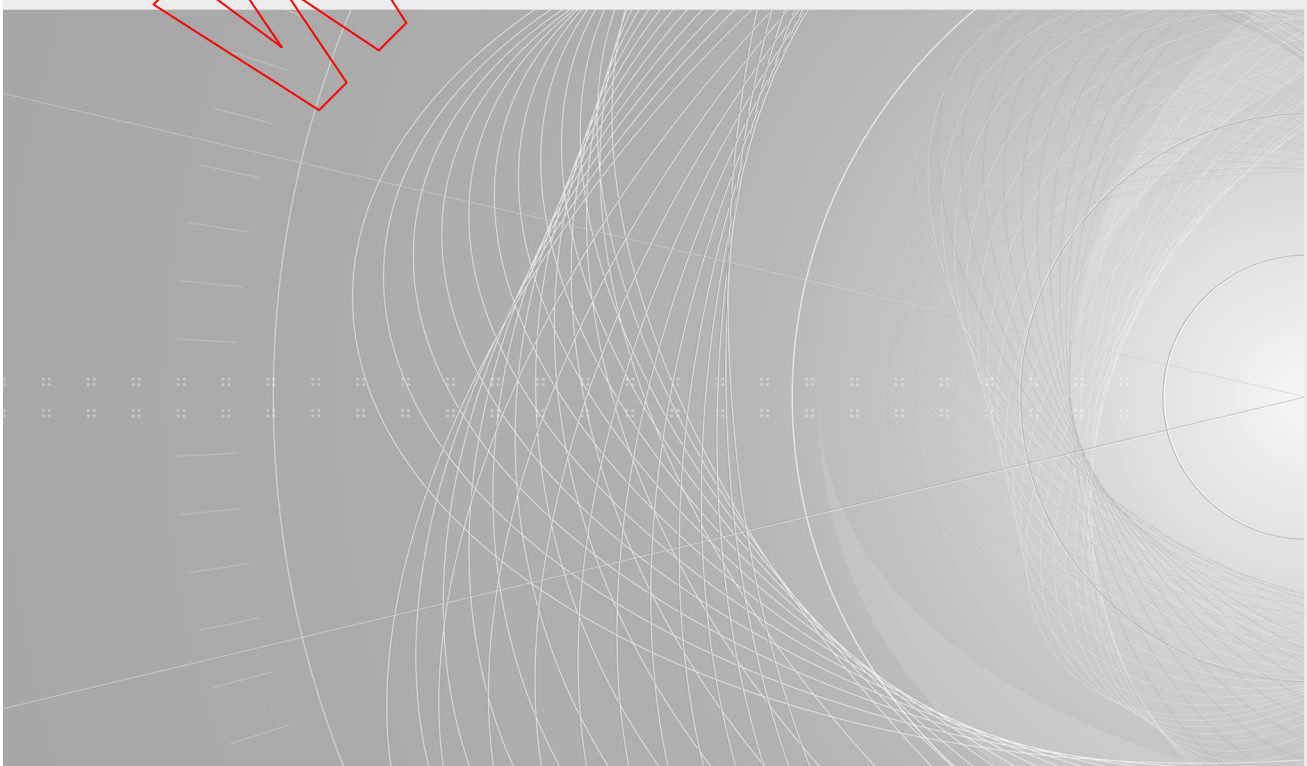
PUBLICLY AVAILABLE SPECIFICATION

PRE-STANDARD

Process management for avionics – Aerospace qualified electronic components (AQEC) –
Part 1: General requirements for high reliability integrated circuits and discrete semiconductors



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INTERNATIONAL ELECTROTECHNICAL COMMISSION

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INTERNATIONAL ELECTROTECHNICAL COMMISSION

PROCESS MANAGEMENT FOR AVIONICS – AEROSPACE QUALIFIED ELECTRONIC COMPONENTS (AQEC) –

Part 1: General requirements for high reliability integrated circuits and discrete semiconductors

FOREWORD

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A PAS is a technical specification not fulfilling the requirements for a standard, but made available to the public.

STACK Specification S/0001 revision 14 *General Requirements for Integrated Circuits and Discrete Semiconductors* has served as a basis for the development of Part 1 of this publicly available specification.

IEC PAS 62686-1 has been processed by IEC technical committee 107: Process management for avionics.

The text of this PAS is based on the following document:	This PAS was approved for publication by the P-members of the committee concerned as indicated in the following document
Draft PAS	**Report on voting**
107/126/PAS	107/136A/RVD

Following publication of this PAS, which is a pre-standard publication, the technical committee or subcommittee concerned may transform it into an International Standard.

This PAS shall remain valid for an initial maximum period of 3 years starting from the publication date. The validity may be extended for a single 3-year period, following which it shall be revised to become another type of normative document, or shall be withdrawn.

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PROCESS MANAGEMENT FOR AVIONICS – AEROSPACE QUALIFIED ELECTRONIC COMPONENTS (AQEC) –

Part 1: General requirements for high reliability integrated circuits and discrete semiconductors

1 Scope

This PAS defines the minimum requirements for general purpose 'off the shelf' COTS integrated circuits and discrete semiconductors for high reliability applications.

This PAS complements IEC/TS 62564-1. IEC/TS 62564-1 is to be used for high reliability applications where additional manufacturer's data is required beyond the publicly available manufacturer published datasheets, e.g. where additional thermal performance data is required for thermally challenging applications or when additional DO-254 verification data is needed for complex components for flight critical applications etc.

This PAS is to be used wherever possible for components that typically can be applied to operate in high reliability applications within the manufacturers publicly available datasheet limits. It is recommended that this PAS be used in conjunction with IEC/TS 62239 for avionics applications.

This PAS is identical to STACK Specification S/0001 revision 14 which is included in Annex A.

NOTE Adoption of the STACK Specification S/0001 revision 14 will enable all existing STACK Certified manufacturers to be audited by IECQ under the new STACK-IECQ joint venture.

2 Normative references

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60695-2-2, *Fire hazard testing – Needle flame test*

IEC 61340-5-1, *Electrostatics – Part 5-1: Protection of electronic devices from electrostatic phenomena – General requirements*

IEC/TS 62239, *Process management for avionics – Preparation of an electronic components management plan*

IEC/TS 62564-1, *Aerospace qualified electronic component (AQEC) – Part 1: Microcircuits*

STACK S/0001 revision 14, *General Requirements for integrated circuits and discrete semiconductors*

EN 100015-3, *Protection of electrostatic sensitive devices. Requirements for clean room areas*

EIA 471, *Symbol and Labels for Electrostatic Sensitive Devices (ESD)*

EIA 541, *Packaging materials for ESD sensitive items*

EIA 556, *Outer shipping container bar code label standard*

JP001.01, *Foundry process qualification guidelines*

JEP119, *Performing Standard Wafer level Electromigration Accelerated |Test (SWEAT)*

JEP130-A, *Guidelines for Packing and Labeling of Integrated Circuits in Unit Container Packing (Tubes, Trays, and Tape and Reel)*

JEP138, *User guidelines for IR thermal imaging determination of die temperature*

JESD6 , *Measurement of small values of transistor capacitance*

JESD22-A101, *Steady state temperature humidity bias life test*

JESD22-A102 , *Accelerated moisture resistance unbiased autoclave*

JESD22-A103 , *High temperature storage life*

JESD22-A104 , *Temperature cycling*

JESD22-A108 , *Temperature bias and operating life*

JESD22-A109 , *Hermeticity*

JESD22-A110 , *Highly accelerated temperature and humidity stress test (HAST)*

JESD22-A113 , *Preconditioning of plastic surface mount devices prior to reliability testing*

JESD22-A114 , *Electrostatic Discharge Sensitivity (ESDS) testing Human Body Model (HBM)*

JESD22-A117 , *Endurance – Program/Erase cycle*

JESD22-A118 , *Accelerated moisture resistance – unbiased HAST*

JESD22-B100 , *Physical Dimension*

JESD22-B101 , *External visual*

JESD22-B102 , *Solderability test method*

JESD22-B103 , *Vibration, variable frequency*

JESD22-B104 , *Mechanical shock*

JESD22-B105, *Lead integrity*

JESD22-B106 , *Resistance to soldering heat*

JESD22-B107 , *Marking permanency*

JESD22-B116 , *Wire bond shear test*

JESD24, *Power MOSFETS*

JESD24-3, *Addendum No 3 to JESD24 – Thermal impedance measurements for vertical power mosfets (delta source-drain voltage method)*

JESD24-4, *Addendum No 4 to JESD24 – Thermal impedance measurements for bipolar transistors (delta base-emitter voltage method)*

JESD28, *Procedure for measuring N-Channel MOSFET hot-carrier degradation at maximum substrate current under DC stress*

JESD282, *Silicon rectifier diodes*

JESD313, *Thermal resistance measurements of conduction cooled power transistors*

JESD36, *Standard Description of Low-Voltage TTL-Compatible, 5 v Tolerant CMOS Logic Devices*

JESD46, *Customer notification of Product/Process changes by Semiconductor Supplier's*

JESD47, *Stress test driven qualification of integrated circuits*

JESD48, *Product Discontinuance*

JESD51-1, *Integrated Circuit Thermal Measurement Method – Electrical Test Method (Single Semiconductor Device)*

JESD51-2, *Integrated circuits thermal test method environmental conditions – natural convection (still air)*

JESD52, *Standard For Description of Low Voltage TTL-Compatible CMOS Logic Devices*

JESD531, *Thermal resistance test method for signal and regulator diodes (forward voltage, switching method)*

JESD625, *Requirements for handling Electrostatic Discharge Sensitive devices*

JESD76, *Description of 1.8 V CMOS Logic Devices*

JESD76-1, *Standard Description of 1.2 V CMOS Logic Devices (Wide Range Operation)*

JESD76-2, *Standard Description of 1.2 V CMOS Logic Devices (Normal Range Operation)*

JESD76-3, *Standard Description of 1.5 V CMOS Logic Devices*

JESD78, *IC Latchup test*

JESD79, *Double Data Rate (DDR) SDRAM Specification*

JESD79-2, *DDR2 SDRAM Specification*

JESD79-3, *DDR3 SDRAM Standard*

JESD80, *Standard for Description of 2.5 V CMOS Logic Devices*

JESD86, *Electrical Parameter Assessment*

JESD89, *Measurement and Reporting of Alpha Particles and Terrestrial Cosmic Ray-Induced Soft Errors in Semiconductor Devices*

JESD94.01, *Application Specific Qualification Using Knowledge Based Test Methodology*

JESD99, *Terms, Definitions and Letter Symbols for Microelectronic Devices*

J-STD-004, *Requirements for soldering fluxes*

J-STD-020, *Moisture/reflow sensitivity classification for non-hermetic solid state surface mount devices*

J-STD-033, *Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices*

J-STD-035, *Acoustic microscopy for non-hermetic encapsulated electronic components*

MIL-STD-883, *Test methods standard microcircuits*

MIL-STD-750, *Test Method standards for semiconductor devices*

UL94, *Flammability of plastic materials for parts in devices and appliances, tests for*

AEC-Q100, *Stress Test Qualification for Integrated Circuit*

AEC-Q101, *Stress Test Qualification for Discrete Semiconductors, Customer Specific Requirements (ISO/TS-16949) Semiconductor Commodity – For use by the Semiconductor Suppliers*

3 Terms, definitions and abbreviations

For the purposes of this document, the following terms, definitions and abbreviations apply. When the following terms are used in *Italics*, they have the meaning defined in this clause.

3.1
calendar days
continuous days, including weekends and holidays

3.2
customer, user
original equipment manufacturer (OEM) who procures integrated circuits and/or semiconductor devices compliant to this PAS and uses them to design, produce, and maintain systems

3.3
data sheet
document prepared by the manufacturer that describes the electrical, mechanical, and environmental characteristics of the component

3.4
deviation
user agreement to allow the delivery of a *shipping lot* which does not fully meet the requirements of this *specification*

Considered equivalent to concession for the purposes of this document.

3.5
device specification
document written by a *user* and agreed by the *supplier*

3.6
form
shape, arrangement of parts, visible aspect, mode in which a part exists or manifests itself, the material an item is constructed from

3.7
fit
qualified and competent; correct size and shape

3.8
function
work to a specification that an item is designed to without degrading reliability

3.9
incoming lot
one or more shipments of a *device,* grouped together for the purpose of incoming inspection

3.10
inner box
a box or bag containing *devices,* either in *magazines* or bulk packaged

3.11
integrated circuit
microcircuit in which all or some of the circuit elements are inseparably associated and electrically interconnected so that it is considered to be indivisible for the purpose of construction and commerce

3.12
limitation
requirement of this specification that is not met

3.13
magazine
sticks, tubes, matrix trays, tape/reel, etc.

3.14
microcircuit, component, device
electrical or electronic device, with a high circuit-element density, in which all or some of the circuit elements are inseparably associated and electrically interconnected (on one or more substrates, in a unique indivisible package) so that it is considered to be indivisible for the purpose of construction and commerce

3.15 outer box
outer shipping container, containing one or more *inner boxes*

3.16
room remperature
temperature of 25 °C ± 5 °C

3.17
semiconductor, device
electronic devices in which the essential electrical characteristic distinguishing electronic conduction takes place due to the flow of charge carriers within one or more semiconductor materials

This includes:

a) semiconductor diodes which are semiconductor devices having two terminals and exhibiting a nonlinear voltage-current characteristic, and

b) transistors which are active semiconductor devices capable of providing power amplification and having three or more terminals.

3.18
shipping lot
single lot of one or more *outer boxes* received by a *user*

3.19
supplier
the company identified by the logo or name marked on the device

3.20
termination
element of a component that connects it electrically and mechanically to the next level of assembly

3.21
triboelectric charge
electrical charge generated by frictional movement or separation of two surfaces

3.22
user
the general public using this IEC specification , STACK Members, IECQ Certification Bodies (CBs) or organizations authorized by the STACK Office to use this specification

3.23
waiver
written notice that a requirement of this *specification* no longer applies or is relaxed as requested during the registration process

If granted by the STACK Members, the *waiver* shall be documented on the Registration Certificate and is applicable to that individual *supplier* only.

4 Abbreviations

AQEC	Aerospace qualified electronic component
BPSG	Borophosphosilicate glass
COTS	Commercial off the shelf
CMOS	Complementary metal oxide semiconductor
DPM	Defects per million. It may also be referred as PPM (parts per million).
DSCC	Defence supply centre Columbus (see http://www.dscc.dla.mil/)

ECMP	Electronic component management plan
FFF	Form, fit and function
FIT	Failures in time
HAST	Highly accelerated stress test
HCI	Hot carrier injection
HTOL	High temperature operating life
LTB	Last time buy
LTPD	Lot tolerance percent defective
MSL	Moisture sensitivity level as defined in J-STD-20 relating to the packaging and handling precautions needed for semiconductors
NBTI	Negative bias temperature instability
PCN	Product change notification
SEE	Single event effect
SEU	Single event upset
SER	Soft error rate
THB	Temperature humidity bias
T_{op}min	Minimum operating temperature
T_{op}max	Maximum operating temperature

5 Technical requirements

The *supplier* shall provide the *user* requirements for quality, reliability and general requirements for integrated circuits and discrete semiconductors not otherwise governed by and supplied to Military Specifications, as stated in STACK S/0001 revision 14. STACK S/0001 specification revision 14 is included in Annex A.

NOTE 1 The required information is available to STACK Members by a method agreed during registration and to IECQ certified companies from their IECQ certification body (IECQ CB).

NOTE 2 Limitations may be identified during a certification audit where some of suppliers products do not meet the requirements of this specification due to marketing reasons. In that event, the supplier shall be noted as having limitations which shall be recorded in the audit report and on the certificate. These limitations are applicable to that individual supplier only.