



JPCA

IEC/PAS 62326-20

Edition 1.0 2011-01

PUBLICLY AVAILABLE SPECIFICATION

PRE-STANDARD



Printed boards –
Part 20: Electronic circuit board for high-brightness LEDs

IEC PAS 62326-20:2011
<https://standards.iteh.ai/catalog/standards/sist/95c024d3-78f7-43d6-99d4-8c51f81f5b03/iec-pas-62326-20-2011>

Without claim



THIS PUBLICATION IS COPYRIGHT PROTECTED

Copyright © 2011 IEC, Geneva, Switzerland

All rights reserved. Unless otherwise specified, no part of this publication may be reproduced or utilized in any form or by any means, electronic or mechanical, including photocopying and microfilm, without permission in writing from either IEC or IEC's member National Committee in the country of the requester.

If you have any questions about IEC copyright or have an enquiry about obtaining additional rights to this publication, please contact the address below or your local IEC member National Committee for further information.

IEC Central Office
3, rue de Varembe
CH-1211 Geneva 20
Switzerland
Email: inmail@iec.ch
Web: www.iec.ch

About the IEC

The International Electrotechnical Commission (IEC) is the leading global organization that prepares and publishes International Standards for all electrical, electronic and related technologies.

About IEC publications

The technical content of IEC publications is kept under constant review by the IEC. Please make sure that you have the latest edition, a corrigenda or an amendment might have been published.

- Catalogue of IEC publications: www.iec.ch/searchpub

The IEC on-line Catalogue enables you to search by a variety of criteria (reference number, text, technical committee,...). It also gives information on projects, withdrawn and replaced publications.

- IEC Just Published: www.iec.ch/online_news/justpub

Stay up to date on all new IEC publications. Just Published details twice a month all new publications released. Available on-line and also by email.

- Electropedia: www.electropedia.org

The world's leading online dictionary of electronic and electrical terms containing more than 20 000 terms and definitions in English and French, with equivalent terms in additional languages. Also known as the International Electrotechnical Vocabulary online.

- Customer Service Centre: www.iec.ch/webstore/custserv

If you wish to give us your feedback on this publication or need further assistance, please visit the Customer Service Centre FAQ or contact us:

Email: csc@iec.ch
Tel.: +41 22 919 02 11
Fax: +41 22 919 03 00



JPCA

IEC/PAS 62326-20

Edition 1.0 2011-01

PUBLICLY AVAILABLE SPECIFICATION

PRE-STANDARD



Printed boards –
Part 20: Electronic circuit board for high-brightness LEDs

<https://standards.iteh.ai/catalog/standards/sist/91e924d3-78f7-43d6-99d4-8c51f81f5b03/iec-pas-62326-20-2011>

INTERNATIONAL
ELECTROTECHNICAL
COMMISSION

PRICE CODE



ICS 31.180

ISBN 978-2-88912-345-2

CONTENTS

FOREWORD.....	6
1 Scope.....	8
2 Terms and definitions.....	8
3 Classification and class of the ECB.....	8
4 Design rules and allowance.....	9
4.1 Panel and board sizes.....	9
4.1.1 Board size (for reference only).....	9
4.1.2 Allowance of dimensions.....	10
4.1.3 Perforation and slit.....	10
4.1.4 V-cut.....	11
4.2 Total board thickness.....	12
4.2.1 Total board thickness and its allowance.....	12
4.3 Holes.....	13
4.3.1 Insertion holes and vias.....	13
4.3.2 Datum hole.....	15
4.3.3 Assembly hole (a through-hole without wall plating).....	15
4.4 Conductor.....	15
4.4.1 Width of conductor pattern and its allowance.....	15
4.4.2 Distance between conductors and its allowance.....	16
4.4.3 Distance between conductor and board edge.....	17
4.4.4 Thickness of the insulating layer.....	17
4.5 Printed contact.....	18
4.5.1 Allowance of the distance between the centres of two adjacent printed contacts.....	18
4.5.2 Allowance of the terminal width of printed contacts.....	18
4.5.3 Shift of the centre of printed contacts on front and back sides of a board.....	18
4.6 Footprint.....	19
4.6.1 Allowance of the distance between the centers of two pads.....	19
4.6.2 Allowance of the width of a pad.....	19
4.6.3 Pad diameter and its allowance for BGA/CSP.....	20
4.7 Fiducial mark and the mark for component positioning.....	21
4.8 Interlayer connection.....	22
5 Quality.....	22
5.1 Gap between conductor and the wall of a component insertion hole or a via.....	22
5.2 Positional deviation between conductor layers of multilayer board.....	22
5.3 Minimum land width.....	22
5.4 Surface treatment.....	24
5.4.1 Gold plating for printed contact.....	24
5.4.2 Other surface treatment.....	24
5.5 Defects of solder resist.....	24
5.6 Symbol mark.....	26
5.7 Appearance.....	27
5.7.1 Conductor surface.....	27
5.7.2 Between conductors.....	27
6 Performance and test methods.....	33

6.1	Observation of component mounting for and vias	33
6.1.1	Observation with standard conditions	33
6.1.2	Observation after thermal shock test	34
7	Marking, packaging and storage	47
7.1	Marking on a product.....	47
7.2	Marking on the package	47
7.3	Packaging and storage	47
7.3.1	Packaging	47
7.3.2	Storage	47
8	Normative references	47
	Annex A (informative) Additional information to IEC/PAS 62326-20.....	48
	Figure 1 – Example of classification and their application by base materials, electronic circuit boards and final products	9
	Figure 2 – Board arrangement in a panel	9
	Figure 3 – Distances from the datum point to perforation and slit.....	10
	Figure 4 – Distance from the datum point to V-cut	11
	Figure 5 – Allowance of position off-set of V-cuts on front and back surfaces	11
	Figure 6 – PWB board with symbol mark, solder resist, copper foil and plating	12
	Figure 7 – Positions of component insertion holes	13
	Figure 8 – Distance between the wall of a hole to the board edge.....	14
	Figure 9 – Hole wall and the minimum designed spacing to the inner conductor.....	15
	Figure 10 – Width of finished conductor.....	16
	Figure 11 – Distance between finished conductors.....	17
	Figure 12 – Thickness of the insulating layer	17
	Figure 13 – Distance between centres of terminals of printed contacts	18
	Figure 14 – Terminal width of a printed contact.....	18
	Figure 15 – Shift of the centre of printed contacts on front and back sides of a board	19
	Figure 16 – Foot print	19
	Figure 17 – Pad width of a footprint	20
	Figure 18 – Allowance of pad diameter of BGA/CSP formed of conductor only.....	20
	Figure 19 – Pad diameter (d) of BGA/CSP formed at the opening of solder resist	21
	Figure 20 – Examples of fiducial mark and component positioning mark	21
	Figure 21-1 – Minimum land width on the outer layer	23
	Figure 21-2 – Minimum land width on the inner layer with a plated through-hole	23
	Figure 21-3 – Allowable area of land break	24
	Figure 22 – Exposure of conductor	25
	Figure 23 – Minimum land width caused by the shift of solder resist	25
	Figure 24 – The overlap, smear and shift of solder resist	26
	Figure 25 – Examples	26
	Figure 26 – Example of measling	27
	Figure 27 – Examples of crazing.....	28
	Figure 28 – Missing of conductor	28
	Figure 29 – Conductor residue.....	28

Figure 30 – Land.....	29
Figure 31 – Defects in a pad of a footprint	29
Figure 32 – Defects in BGA/CSP mounting pads.....	30
Figure 33 – The areas to be checked for defects of a printed contact.....	31
Figure 34 – Defects in a printed contact.....	31
Figure 35 – Defect on a plating of a component mounting hole	33
Figure 36-1 – Resin smear.....	34
Figure 36-2 – Corner crack	35
Figure 36-3 – Barrel crack	35
Figure 36-4 – Foil crack	35
Figure 37 – The relations between resistance and width, thickness and temperature of conductor.....	36
Figure 38 – Temperature rise as functions of width and thickness of conductor and current.....	37
Table 1 – Application and classification	8
Table 2 – Panel dimensions (informative purpose).....	10
Table 3– Allowance of dimensions	10
Table 4 – Allowance of the distances from the datum point to perforation and slit	11
Table 5 – Allowance for the distance from the datum point to the center of the V-cut	12
Table 6 – Total thickness and its allowance.....	12
Table 7 – Allowance of holes for component insertion.....	13
Table 8 – Position allowance of component insertion holes.....	13
Table 9 – Distance between a hole wall and board edge.....	14
Table 10 – Minimum clearance between the hole wall and the inner layer conductor.....	14
Table 11 – Allowance of conductor width	16
Table 12 – Allowance of the distance between conductors.....	16
Table 13 – Distance between conductor and board edge	17
Table 14 – Allowance of the terminal width of a printed contact	18
Table 15 – Allowance of the distance between the centres of two pads.....	19
Table 16 – Allowance of the width of a pad of a footprint	20
Table 17 – Pad diameter and its allowance for BGA/CSP.....	20
Table 18 – Allowance of the pad diameter (d) of BGA/CSP formed at the opening of solder resist.....	21
Table 19 – Shapes and sizes of typical fiducial marks and component positioning marks	22
Table 20 – Minimum thickness of copper plating	22
Table 21 – Minimum land width.....	23
Table 22 – Minimum land width.....	25
Table 23 – The overlap, smear and shift of solder resist over a fool print.....	26
Table 24 – Allowance of the area of a defect, remaining width and protrusion of a land	29
Table 25 – Defect of a pad of a footprint	30
Table 26 – Defects in BGA/CSP mounting pads	30
Table 27 – Defects in a printed contact.....	32

Table 28 – Allowance in horizontal sectioning	34
Table 29 – Specification and test methods	38
Table A.1 – The relation between thermal conductive parameter (W/(mK)) and heat transfer coefficient parameter	49
Table A.2 – The relation between thermal conductive parameter (W/(mK)) and heat transfer coefficient parameter	49

Withhold

iTeh STANDARD PREVIEW
(standards.iteh.ai)

IEC PAS 62326-20:2011
<https://standards.iteh.ai/catalog/standards/sist/91e024d3-78f7-43d6-99d4-8c51f81f5b03/iec-pas-62326-20-2011>

INTERNATIONAL ELECTROTECHNICAL COMMISSION

PRINTED BOARDS –

Part 20: Electronic circuit board for high-brightness LEDs

FOREWORD

- 1) The International Electrotechnical Commission (IEC) is a worldwide organization for standardization comprising all national electrotechnical committees (IEC National Committees). The object of IEC is to promote international co-operation on all questions concerning standardization in the electrical and electronic fields. To this end and in addition to other activities, IEC publishes International Standards, Technical Specifications, Technical Reports, Publicly Available Specifications (PAS) and Guides (hereafter referred to as "IEC Publication(s)"). Their preparation is entrusted to technical committees; any IEC National Committee interested in the subject dealt with may participate in this preparatory work. International, governmental and non-governmental organizations liaising with the IEC also participate in this preparation. IEC collaborates closely with the International Organization for Standardization (ISO) in accordance with conditions determined by agreement between the two organizations.
- 2) The formal decisions or agreements of IEC on technical matters express, as nearly as possible, an international consensus of opinion on the relevant subjects since each technical committee has representation from all interested IEC National Committees.
- 3) IEC Publications have the form of recommendations for international use and are accepted by IEC National Committees in that sense. While all reasonable efforts are made to ensure that the technical content of IEC Publications is accurate, IEC cannot be held responsible for the way in which they are used or for any misinterpretation by any end user.
- 4) In order to promote international uniformity, IEC National Committees undertake to apply IEC Publications transparently to the maximum extent possible in their national and regional publications. Any divergence between any IEC Publication and the corresponding national or regional publication shall be clearly indicated in the latter.
- 5) IEC itself does not provide any attestation of conformity. Independent certification bodies provide conformity assessment services and, in some areas, access to IEC marks of conformity. IEC is not responsible for any services carried out by independent certification bodies.
- 6) All users should ensure that they have the latest edition of this publication.
- 7) No liability shall attach to IEC or its directors, employees, servants or agents including individual experts and members of its technical committees and IEC National Committees for any personal injury, property damage or other damage of any nature whatsoever, whether direct or indirect, or for costs (including legal fees) and expenses arising out of the publication, use of, or reliance upon, this IEC Publication or any other IEC Publications.
- 8) Attention is drawn to the Normative references cited in this publication. Use of the referenced publications is indispensable for the correct application of this publication.
- 9) Attention is drawn to the possibility that some of the elements of this IEC Publication may be the subject of patent rights. IEC shall not be held responsible for identifying any or all such patent rights.

A PAS is a technical specification not fulfilling the requirements for a standard, but made available to the public.

IEC-PAS 62326-20 was submitted by the JPCA (Japan Electronics Packaging and Circuits Association) and has been processed by IEC technical committee 91: Electronics assembly technology.

It is based on JPCA-TMC-LED01S-2010. It is published as a double-logo PAS and JPCA.

The text of this PAS is based on the following document:

This PAS was approved for publication by the P-members of the committee concerned as indicated in the following document

Draft PAS	Report on voting
91/926/PAS	91/942A/RVD

Following publication of this PAS, which is a pre-standard publication, the technical committee or subcommittee concerned may transform it into an International Standard.

This PAS shall remain valid for an initial maximum period of 3 years starting from the publication date. The validity may be extended for a single period up to a maximum of 3 years, at the end of which it shall be published as another type of normative document, or shall be withdrawn.

A list of all the parts in the IEC 62326 series, under the general title *Printed boards*, can be found on the IEC website.

IMPORTANT – The 'colour inside' logo on the cover page of this publication indicates that it contains colours which are considered to be useful for the correct understanding of its contents. Users should therefore print this document using a colour printer.

IEC PAS 62326-20:2011

<https://standards.iec.ch/catalog/standards/sst/91/926-24d3-78f7-43d6-99d4-8c51f81f5b03/iec-pas-62326-20-2011>

PRINTED BOARDS –

Part 20: Electronic circuit board for high-brightness LEDs

1 Scope

This PAS specifies the properties of the electronic circuit board for high-brightness LEDs (hereafter described as “ECB”).

NOTE Standards relevant to the present standards are given below.

JPCA-TD01 Terms and definitions for printed circuits

JIS C 5603 Terms and definitions for printed circuits

2 Terms and definitions

For the purpose of this document, the terms used in this PAS shall be in accordance with JPCA-TD01 and JIS C 5603, unless otherwise specified.

3 Classification and class of the ECB

The ECB specified in this PAS shall satisfy the specification of (A) to (C) in Table 1 in the following way. The materials used in the materials of RWB are not specified; however, they shall be agreed upon between user and supplier depending on the application area of the boards in question.

Table 1 – Application and classification

Classification (thermal conductivity)	Definition	Small classification (insulation property)	Definition	Thermal conductivity parameter W/(mK)	Heat transfer parameter W/(m ² K)
A	Standard boards	I	No specification	<1	<10
		II	Electric strength <1,000 V		
		III	Electric strength 1,000 V≤		
B	Thermal conductive boards	I	No specification	1≤	<10
		II	Electric strength <1,000 V		
		III	Electric strength 1,000 V≤		
C	High thermal conductive boards	I	No specification	1≤	10≤
		II	Electric strength <1,000 V		
		III	Electric strength 1,000 V≤		

Heat Radiation	A			B			C				
Classification by base materials	Resin type substrate (CEM-3, FR-4, FR-5)			Resin type substrate (with thermal via)			Metal core substrate				
	Flexible type substrate			High thermal conductive resin substrate							
Classification by electronic circuit boards	Conventional substrate for discrete type electronic parts mounted boards										
	Substrate for semiconductor package										
	Substrate for Chip on Board										
Classification by final products	Assistant lighting lamp			Lamp substitute for halogen lamp			Street lamp				
				Lamp substitute for fluorescent lamp substitute							
				Lamp substitute for filament lamp							
				Lamp substitute for HID							
Insulation class			I	II	III	I	II	III	I	II	III

Figure 1 – Example of classification and their application by base materials, electronic circuit boards and final products

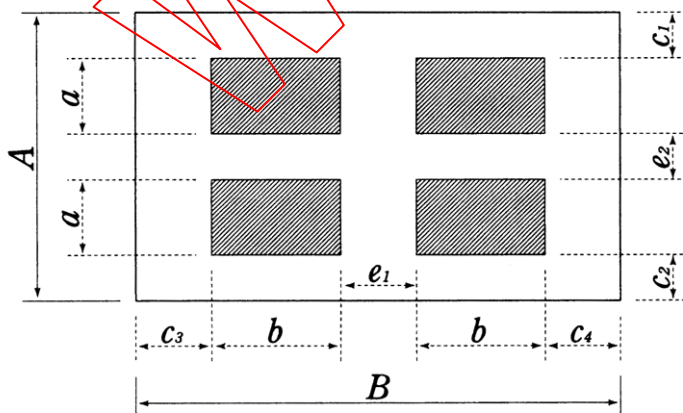
4 Design rules and allowance

4.1 Panel and board sizes

4.1.1 Board size (for reference only)

The size of the board of the product (a x b) illustrated in Figure 2 shall be selected so that the boards can be arranged efficiently within a panel with a size specified in Table 2. Or, a proper panel with a size given in the table shall be selected so as to satisfy the required efficient arrangement of the boards.

Table 1. PWB



Board size of the product: a x b
 Space between board and panel edges: c₁, c₂, c₃, c₄
 Space between boards: e₁, e₂

Figure 2 – Board arrangement in a panel

Table 2 – Panel dimensions (informative purpose)

Size of CCL (copper clad laminate) panel	Division			
	4	6	8	9
1 000 × 1 000	500 × 500	333 × 500	250 × 500	333 × 333
1 000 × 1 200	500 × 600	333 × 600 400 × 500	300 × 500	333 × 400

4.1.2 Allowance of dimensions

The allowance of dimensions of a board or a panel is given in Table 3.

Table 3– Allowance of dimensions

Longitudinal size	Allowance
≤ 100	±0,2
100<	Add 0,1 for each 50 exceeding a length of 100.

4.1.3 Perforation and slit

The perforation and slit are shown in Figure 3. The allowance of the distances from the datum point to the center of the cut of the perforation and slit is given in Table 4.

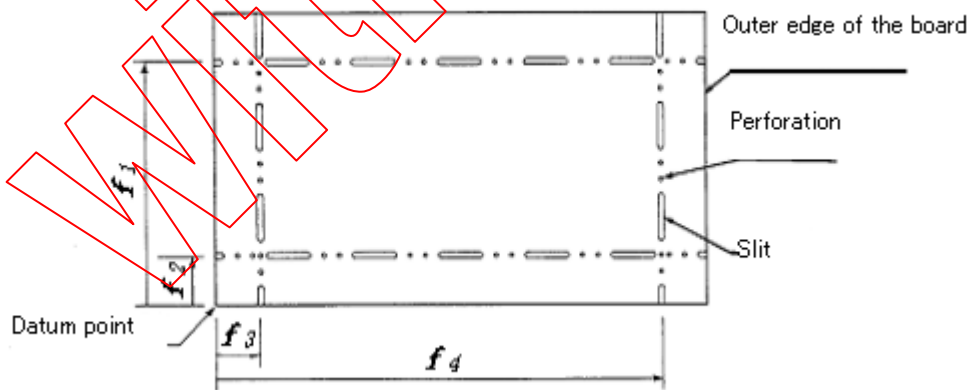


Figure 3 – Distances from the datum point to perforation and slit

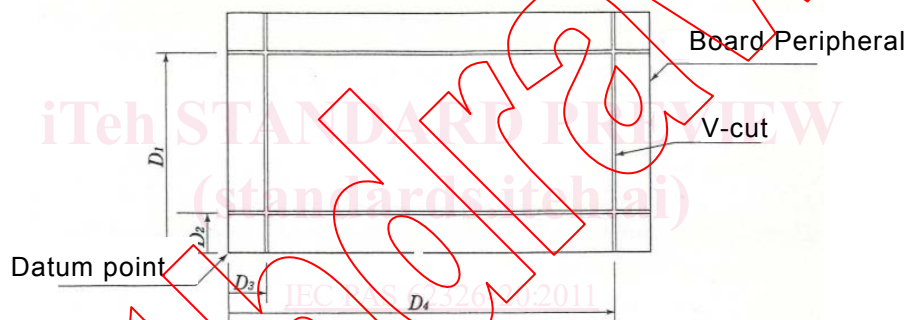
Table 4 – Allowance of the distances from the datum point to perforation and slit

Distances from the datum point to perforation and slit	Allowance
≤ 100	$\pm 0,2$
$100 <$	Add 0,1 for each 50 beyond a length of 100.

mm

4.1.4 V-cut

The V-cut is shown in Figure 4. The allowance of the distance from the reference datum to the center of cut of the V (g_1 to g_4) is given in Table 5. The allowance of the deviation of the position of the V-cut on the front and back planes is 0,2 mm, and the allowance of the uncut thickness of the board is the sum of the allowance of the board thickness $\pm 0,1$ mm.

**Figure 4 – Distance from the datum point to V-cut**

mm

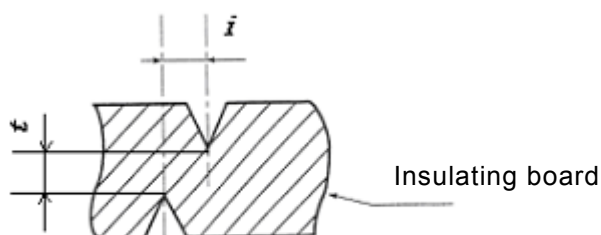
**Figure 5 – Allowance of position off-set of V-cuts on front and back surfaces**

Table 5 – Allowance for the distance from the datum point to the center of the V-cut

Distance from the datum point to the center of the V-cut	Allowance
≤100	±0,2
>100	Add 0,1 for each 50 mm exceeding a length over 100 mm

4.2 Total board thickness

4.2.1 Total board thickness and its allowance

The allowance of the total board thickness (*t*) of a board with solder resist and symbol marks as shown in Figure 6 is given in Table 6.

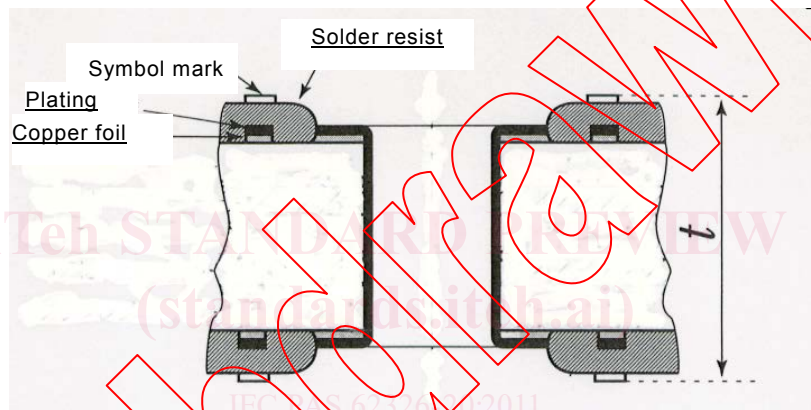


Figure 6 – PWB board with symbol mark, solder resist, copper foil and plating

Table 6 – Total thickness and its allowance

Total thickness (center value of the final board) mm	Allowance
≤ 0,3 to < 0,5	+ 0,10 - 0,05
≤ 0,5 to < 0,8	±0,10
≤ 0,8 to < 1,10	±0,15
≤ 1,10 to < 1,40	±0,17
≤ 1,40 to < 2,00	±0,19
≤ 2,00	±10 %

4.3 Holes

4.3.1 Insertion holes and vias

(1) Allowance of component insertion holes

Allowance of component insertion holes is given in Table 7. The allowance given in this table is not applicable to vias (through-hole vias, buried vias and blind vias). The allowance of through-holes with a diameter less than 0,6 mm for insertion of a component and holes for press-fit of a component is to be agreed between user and supplier.

Table 7 – Allowance of holes for component insertion

Item		Allowance
Plated through-hole	0,6 ≤ <2,0	±0,10
	2,0 ≤	±0,15
Non-plated through-hole		±0,10

mm

(2) Position of a hole for component insertion

The center of a hole for component insertion should be at the cross point of the grid for pattern design including the complementary grid lines used. The allowance of a component insertion hole position, $(| \vec{r}, j |)$, the deviation from the designed position in respect to the datum point as shown in Figure 7 is given in Table 8.

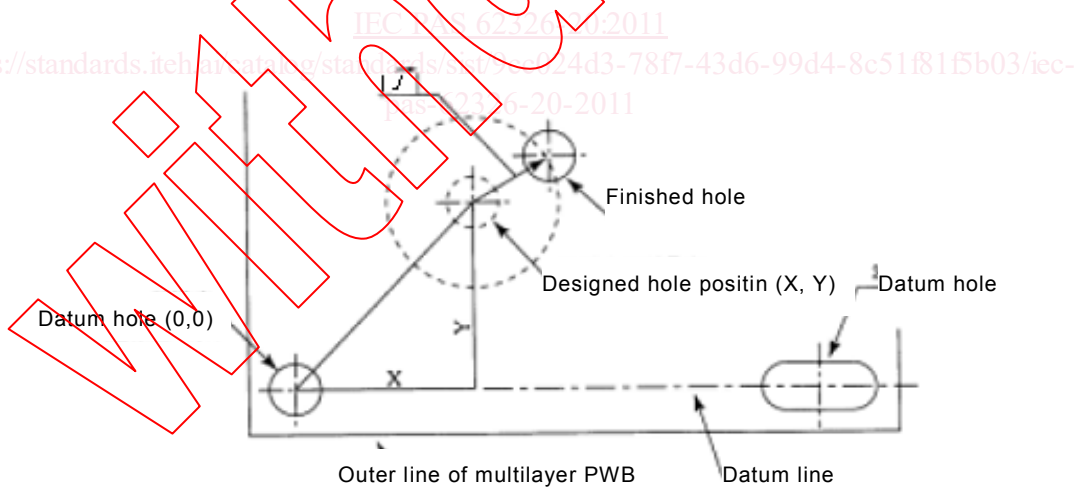


Figure 7 – Positions of component insertion holes

Table 8 – Position allowance of component insertion holes

Longer dimension of rectangular board	Allowance
≤ 400	0,10
400<	For board exceeding 400, add 0,05 for each additional 100

mm