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Information technology – Microprocessor systems – Futurebus+ – Logical protocol specification

Technologies de l'information – Systèmes à microprocesseurs – Futurebus+ – Spécification du protocole logique

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Abstract: This International Standard provides a set of tools with which to implement a Futurebus+ architecture with performance and cost scalability over time, for multiple generations of single- and multiple-bus multiprocessor systems. Although this specification is principally intended for 64-bit address and data operation, a fully compatible 32-bit subset is provided, along with compatible extensions to support 128- and 256-bit data highways. Allocation of bus bandwidth to competing modules is provided by either a fast centralized arbiter, or a fully distributed, one or two pass, parallel contention arbiter. Bus allocation rules are provided to suit the needs of both real-time (priority based) and fairness (equal opportunity access based) configurations. Transmission of data over the multiplexed address/data highway is governed by one of two intercompatible transmission methods: a) a technology-independent, compelled-protocol, supporting broadcast, broadcall, and transfer intervention (the minimum requirement for all Futurebus+ systems), and b) a configurable transfer-rate, source-synchronized protocol supporting only block transfers and source-synchronized broadcast for systems requiring the highest possible performance. Futurebus+ takes its name from its goal of being capable of the highest possible transfer rate consistent with the technology available at the time modules are designed, while ensuring compatibility with all modules designed to this standard both before and after. The plus sign (+) refers to the extensible nature of the specification, and the hooks provided to allow further evolution to meet unanticipated needs of specific application architectures. It is intended that this International Standard be used as a key component of an approved IEEE Futurebus+ profile.

Keywords: bus architecture, Futurebus+, logical protocol, multiprocessor systems

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Information technology—Microprocessor systems—Futurebus+ — Logical protocol specification

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In 1993, ANSI/IEEE Std 896.1-1991, together with IEEE Std 896.1a-1993, *Errata, Corrections and Clarifications*, was adopted by ISO/IEC JTC 1, as draft International Standard ISO/IEC DIS 10857. This edition incorporates IEEE Std 896.1a-1993 into the text of ANSI/IEEE Std 896.1-1991.

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(This introduction is not a normative part of ISO/IEC 10857 : 1994, but is included for information only.)

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IEEE Std 896.1-1991 was approved by the American National Standards Institute on April 28, 1992.

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Information technology—Microprocessor systems—Futurebus+ — Logical protocol specification

1. Overview

1.1 Scope

This International Standard specifies the logical (relative timing and behavioral protocol) layer for a set of signal lines that constitute a multiple segment bus architecture, and for the interfacing of modules connected to a bus segment. This International Standard is intended to be used as a component within a profile (a collection of related specifications that must be used together by a product in order to claim conformance to a standard) to build systems with higher levels of compatibility.

Futurebus+ provides the means for the transfer of binary information between boards over one or more logical buses. Boards may contain any combination of one or more processors and local resources such as cache, memory, peripheral and communication controllers, etc. Figure 1 shows a block diagram of a typical application of Futurebus+.

Protocols are specified for the allocation of bus time to modules that need to conduct transactions with other modules over the bus. However, this International Standard does not mandate the priority rules for modules to use when competing for use of the bus. These are considered the privilege and responsibility of the system integrator. The International Standard includes a complete set of signaling rules to be followed by all modules in both the distributed and centralized control acquisition processes leading to bus mastership (clauses 4 and 5). The International Standard also gives a comprehensive set of signaling rules for all modules participating in a bus transaction (clause 6).

Most of the transfer protocols in this International Standard are *compelled*; that is, they are governed by a pure cause-and-effect relationship. This is what gives this International Standard its technology-independent nature. The compelled signaling provides a designer with a logical simplicity for what takes place in the protocols. As a result, there will be maximum compatibility between products designed to this International Standard throughout its operational lifetime.

With any bus, there is the dilemma of how much the standard should specify. There must be a balance between ensuring that all boards designed by a variety of manufacturers can operate together, while not restricting the users of the bus to any preconceived system design. Although the scope of this International Standard has been restricted to exclude many of the system requirements associated with bus-based computer systems, these are being addressed in companion standards.

The common control and register interface to this series of standards for the Futurebus+, and to other proposed IEEE standards (in particular, IEEE Std 1596-1992 [B12][1], IEEE P1014.1 [B2], and IEEE

[1] The numbers in brackets correspond to those of the bibliography in annex A.

P1394 [B11]), is embodied in the unified CSR architecture standard, IEEE Std 1212-1991 [B7], along with a unified DMA architecture for moving data around a system without the need to pass through a processor (IEEE Std 1212.1-1993 [B8]).

This set of protocols has been designed to be as close to technology-independent as possible while maintaining a very high level of efficiency and performance. The bus signals may be implemented using any technology (TTL, Backplane Transceiver Logic, ECL, CMOS, GaAs, etc.) so long as the Futurebus+ signaling conditions are met (incident wave switching on the transmission-line signaling environment, along with the constraints on skew, crosstalk, and transmission reliability). However, in the interest of maximum compatibility between product families, implementations are expected to be associated with one or more IEEE Futurebus+ profiles, which specify the physical layer and set of transactions to suit a particular family of applications.

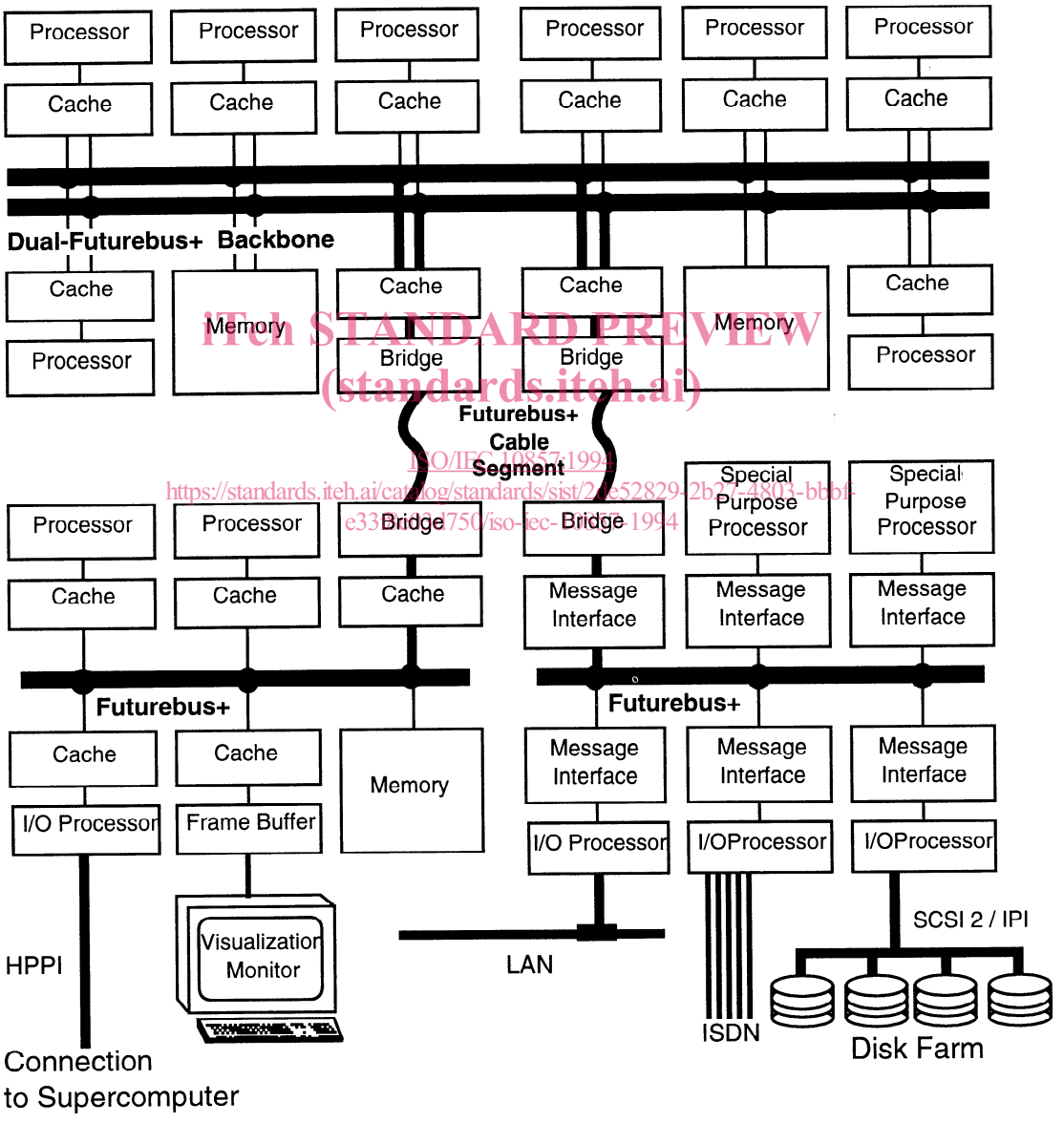

Figure 1—Interfaces in a family of typical Futurebus+ systems

1.2 Normative references

The following standards contain provisions which, through references in this text, constitute provisions of this International Standard. At the time of publication, the editions indicated were valid. All standards are subject to revision, and parties to agreements based on this International Standard are encouraged to investigate the possibility of applying the most recent edition of the standards listed below. Members of IEC and ISO maintain registers of currently valid International Standards.

IEEE Std 896.2-1991, IEEE Standard for Futurebus+ — Physical Layer and Profile Specifications.[2]

IEEE Std 896.3-1993, IEEE Recommended Practices for Futurebus+.[3]

[2] IEEE publications are available from the Institute of Electrical and Electronics Engineers, 445 Hoes Lane, P.O. Box 1331, Piscataway, NJ 08855-1331, USA.

[3] As this standard goes to press, IEEE Std 896.3-1993 is not yet published. It is, however, available in manuscript form from IEEE. Anticipated publication date is May 1994.

2. Definitions and structure

2.1 Special word usage

2.1.1 may: A keyword indicating flexibility of choice with no implied preference.

2.1.2 shall: A keyword indicating a mandatory requirement. Designers must implement all such mandatory requirements to ensure interoperability of ISO/IEC 10857 conformant products and claim conformance to this International Standard.

2.1.3 should: A keyword indicating flexibility of choice with a strongly preferred implementation. The phrase *it is recommended* is used interchangeably with the keyword *should*.

2.2 Definitions

2.2.1 activate: a) The action of applying a set of signals to a group of bus lines. b) The state of a group of bus lines when they carry signals.

2.2.2 address-only transaction: A bus transaction that does not include a data phase. The only information transferred is contained within the connection phase and, in some cases, the disconnection phase.

2.2.3 arbitration: The process of selecting the next bus master.

2.2.4 arbitrated message: A number broadcast on the arbitrated message bus lines to all modules on the bus.

2.2.5 assert: a) The action of applying a logic one signal to a bus line. b) The state of a bus line when the signal it carries represents a logic one.

2.2.6 * (asterisk): When appended to a signal's name, the suffix "*" indicates that the logic one state of the signal is such that it will override the logic zero state applied by any other module on that line.

2.2.7 beat: An event that begins with the transition on a synchronization line by the master, followed by the release of an acknowledge line by one or more slaves. Command and data information may be transferred from the master to one or more slaves in the first half of the beat. During the second half of the beat the slaves may transfer capability, status, and data information back to the master.

2.2.8 block copy: A block copy operation is characterized by a long series of read or write transactions to sequential memory locations.

2.2.9 bus bridge: A bus bridge is an interconnect between two or more buses that provides signal and protocol translation from one bus to another. The buses may adhere to different bus standards for mechanical, electrical, and logical operation (such as a bus bridge from Futurebus+ to VMEbus or to MULTIBUS II).

2.2.10 bus line: The medium for the transmission of signals. Since Futurebus+ requires drivers with wire-OR capability, a bus line may be driven by several modules simultaneously. Therefore, the signal carried by the bus line is the combination of signals applied to that line from each module.

2.2.11 bus tenure: The duration of a master's control of the bus; i.e., the time during which a module has the right to initiate and execute bus transactions.

2.2.12 bus transaction: An event initiated with a connection phase and terminated with a disconnection phase. Data may or may not be transferred during a bus transaction. *See:* **transaction.**

2.2.13 busy: If a slave is unable to accept a bus transaction from a master, it may issue a busy status to the master of the transaction. The master must relinquish the bus and may reacquire the bus and retry the transaction after a suitable time interval.

2.2.14 byte: A set of eight adjacent binary digits.

2.2.15 byte lane: A data path formed by eight data lines and one parity line and used to carry a single byte between system modules.

2.2.16 cache coherence: A system of caches is said to be coherent with respect to a cache line if each cache and main memory in the coherence domain observes all modifications of that same cache line. A modification is said to be observed by a cache when any subsequent read would return the newly written value.

2.2.17 cache memory: A buffer memory inserted between one or more processors and the bus, used to hold currently active copies of blocks from main memory. Cache memories exploit spatial locality by what is brought into a cache. Temporal locality is exploited by the strategy employed for determining what is removed from the cache.

2.2.18 coherence domain: A region in a multiple-cache system, inside of which, cache consistency measures are enforced. In a system that contains bus bridges, a coherence domain may or may not be extensible beyond the local bus through a bus bridge to remote buses.

2.2.19 coherence line: A data block for which cache consistency attributes are maintained.

2.2.20 compelled data transfer protocol: A technology-independent transfer mechanism in which the slave is compelled to provide a response before the master proceeds to the next transfer.

2.2.21 competitor: A module actively participating in the current control acquisition cycle of the arbitration process.

2.2.22 connected transaction: A transaction in which both the request and response are performed within the same bus transaction.

2.2.23 connection phase: A beat that begins with the assertion of the address synchronization line followed by the release of an address acknowledge line. It is used to broadcast the address and command information. Modules determine whether they wish to take part in the transaction based on this information.

2.2.24 control acquisition: The total of all bus activity associated with acquiring exclusive control of the bus.

2.2.25 copyback cache: A cache memory scheme with the attribute that data written from the processor is normally written to the cache rather than the main memory. Modified data in the cache is written to the main memory to avoid loss of the data when a cache line flush or replacement occurs.

2.2.26 CSR: Control and status register.

2.2.27 CSRA: Control and status register architecture. (See IEEE Std 1212-1991 [B7].)

2.2.28 data phase: A period within a transaction used to transfer data.