INTERNATIONAL STANDARD

ISO/IEC 10861

ANSI/IEEE Std 1296

First edition
1994-04-27

Information technology— Microprocessor systems— High-performance synchronous 32-bit bus: MULTIBUS II

Technologies de l'information – Systèmes à microprocesseurs – Bus 32 bits synchrone à haute performance: MULTIBUS II

Reference number
ISO/IEC 10861 : 1994(E)
ANSI/IEEE
Std 1296, 1994 Edition

Abstract: The operation, functions, and attributes of a parallel system bus (PSB), called MULTIBUS II, are defined. A high-performance backplane bus intended for use in multiple processor systems, the PSB incorporates synchronous, 32-bit multiplexed address/data, with error detection, and uses a 10 MHz bus clock. This design is intended to provide reliable state-of-the-art operation and to allow the implementation of cost-effective, high-performance VLSI for the bus interface. Memory, I/O, message, and geographic address spaces are defined. Error detection and retry are provided for messages. The message-passing design allows a VLSI implementation, so that virtually all modules on the bus will utilize the bus at its highest performance—32 to 40 Mbyte/s. An overview of PSB, signal descriptions, the PSB protocol, electrical characteristics, and mechanical specifications are covered.
Keywords: high-performance synchronous 32-bit bus, MULTIBUS II, system bus architectures

The Institute of Electrical and Electronics Engineers, Inc.
345 East 47th Street, New York, NY 10017-2394, USA

ISBN 1-55937-368-7

April 27, 1994 *SH16766*

ISO/IEC 10861 : 1994
[ANSI/IEEE Std 1296, 1994 Edition]

Information technology—Microprocessor systems—High-performance synchronous 32-bit bus: MULTIBUS II

Sponsor

Technical Committee on Microprocessors and Microcomputers of the IEEE Computer Society

Adopted as an International Standard by the International Organization for Standardization and by the International Electrotechnical Commission

Published by The Institute of Electrical and Electronics Engineers, Inc.

Foreword

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In 1990, ANSI/IEEE Std 1296-1987 was adopted by ISO/IEC JTC 1, as draft International Standard ISO/IEC/DIS 10861. This draft was subsequently approved by ISO/IEC JTC 1 in the form of this edition, which is published as International Standard ISO/IEC 10861 : 1994.

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Introduction

(This introduction is not a normative part of ISO/IEC 10861 : 1994 [ANSI/IEEE Std 1296, 1994 Edition], but is included for information only.)

In the last decade, the avalanche of new microcomputer technology, especially VLSI, threatened to obsolete products almost before they went into production. To buffer users from this onrush of technology, Intel helped develop standard interfaces. One of the most notable was the MULTIBUS I system bus, which was used as the basis for a standard by the IEEE in 1983 as IEEE Std 796-1983 (after going through a 5-year review and revision process).

In the early 1980s, Intel recognized that the trends toward multiprocessing and more sophisticated microcomputer-based systems called for an advanced 32-bit system bus architecture. Intel called this new bus MULTIBUS II. In continuing to pioneer the open systems technology, which included multiprocessing, four critical requirements were observed: technical credibility, processor independence, standardization, and openness to all levels of integration. Early in the development of the new bus, Intel established a "MULTIBUS II Development Consortium." The consortium gave the new bus a technical credibility that few buses, especially those defined only among board vendors, can match. The companies in the consortium also represented all microprocessor families; included in the group were 68020, 32032, 80386, and Z8000 board and system users, thus ensuring that the bus is easily adaptable to virtually any manufacturer's processor.

The primary benefits being sought in the creation of this new bus were high-performance multiprocessing, high system reliability, ease-of-use by system designers, and improved cost/performance.

Specific bus features were developed in response to these objectives. The 32 Mbyte/s message passing of the bus provides a bus that acts like a very high-speed network connection for multiple processors (or processor equivalents). There is a recognition that the bus is no longer to interconnect a CPU with its memory and I/O; instead the bus is to interconnect whole stand-alone processors with each other and with intelligent "subsystems-on-a-board."

System reliability is enhanced by the features of bus parity, synchronous operation, negative acknowledge, transfer retries, geographic addressing, and advanced backplane design. Ease-of-use by system designers is implemented primarily through the geographic addressing, which provides for dynamic system configuration. The bus encourages the use of software programmable configuration options (and discourages any use of mechanical jumpers). The standardization of the high-level message-passing protocol also gives the system designer an easy-to-use capability for interprocessor communication.

The cost/performance objective of the bus is delivered through its specification of a realizable 32 to 40 Mbyte/s bus bandwidth. Virtually all boards designed to the bus can achieve this bus utilization factor due to the high-level protocol called out in the specification, and thus the availability of standard, high-performance and cost-effective VLSI components to actually implement this level of performance. For example, this specification and the VLSI make it possible for eight concurrent 4 megabyte/second transfers to take place on the bus. This, or other combinations of transfers that add up to 32 Mbyte/s, demonstrate the real cost/performance advantages of the bus for multiprocessor applications.

In 1983 MULTIBUS II was introduced to the IEEE standards process as a part of the considerations for the P896 (Future Bus) working group activities. In the 1984/1985 time frame the MSC (Microcomputer Standards Committee, of the TCMM) formed an independent study group for MULTIBUS II. During this time the many active participants of the group proceeded to thoroughly review and make changes to the proposed draft. In early 1986 the group was assigned a formal project number P1296. During the remainder of 1986, the draft was passed by the Working Group and the MSC after thorough review, discussion, and changes. In 1987, the draft was presented for Sponsor ballot and, after passing, presented to the June 1987 meeting of the IEEE Standards Board.

The IEEE Standards Board calls attention to the fact that there are patents claimed and/or pending on many aspects of this bus by Intel Corporation. IEEE takes no position with respect to patent validity. Intel Corporation has assured the IEEE that it is willing to grant a license for these patents on reasonable and nondiscriminatory terms to anyone wishing to obtain such a license. The general terms of the license are a one-time administration fee of $100 for a nonexclusive perpetual license. Intel Corporation's undertakings in this respect are on file obtained from the legal department of Intel Corporation whose address is Intel Corporation, 5200 N.E. Elam Young Parkway, Hillsboro, OR 97124.

There were many contributors to the standards review process, but the following members deserve special mention for their active participation:

Task Force Coordinators:	Jack Blevins
	Maurice Hubert
	Hubert Kirrmann
	Jim Nebus
Secretary of Working Group:	Steve Cooper
Original Study Group Chairman:	Paul Borrill
Original Draft Editor:	Scott Tetrick

The P1296 Working Group that prepared this standard had the following membership:

Richard W. Boberg, *Chair*

Web Augustine	Gene Freehauf	Ken Smith
Jack Blevins	Maurice Hubert	Michael Thompson
Paul Borrill	Hubert Kirrmann	Scott Tetrick
Steve Cooper	Klaus Mueller	Eike Waltz
Tom Crawford	Jim Nebus	Janusz Zalewski
	Don Nickel	

The following members of the Technical Committee on Microprocessors and Microcomputers were on the balloting body:

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Matt Biewer	Tom Harkaway	Shlomo Pri-Tal
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Jim Flournoy	Gary Nelson	Andrew Wilson
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When the IEEE Standards Board approved this standard on June 11, 1987, it had the following membership:

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IEEE Std 1296-1987 was approved by the American National Standards Institute on February 8, 1987 and was reaffirmed by IEEE on March 17, 1994.

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1. General overview

1.1 Scope

This International Standard defines the operation, functions, and attributes of the IEEE 1296 bus standard.

a) This standard defines a high-performance 32-bit synchronous bus standard.
b) The bus standard must have a design-in lifetime of 10 years with backward compatibility.
c) The standard is intended for general purpose applications to optimize block transfers, including protocol for message passing. For real-time applications, the bus will provide a means of ensuring an upper limit to message delivery time.
d) The standard is intended to be compatible with existing IEC mechanical standards (IEC Pub 297-1,[1] 297-3, and 603-2) with recognition of the need for special front panels to address ESD, EMI, and RFI requirements.
e) Options within the standard will be clearly identified.
f) The standard is intended to support multiple processor modules in a functionally partitioned configuration and heterogeneous processor types in the same system.
g) The standard is intended to support heterogeneous processor types in the same system.
h) Message-passing format and protocol is intended for future migration to a serial system bus.

1.2 Normative references

The following standards contain provisions which, through references in this text, constitute provisions of this International Standard. At the time of publication, the editions indicated were valid. All standards are subject to revision, and parties to agreements based on this International Standard are encouraged to investigate the possibility of applying the most recent edition of the standards listed below. Members of IEC and ISO maintain registers of currently valid International Standards.

DIN 41612, Two Part Connectors for Printed Board, GRIB, to 54 mm, Common Mounting Features, Survey of Types.[2]

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[1] Information on references can be found in 1.2.

[2] DIN publications are available from the Deutsches Institut für Normung, Burggrafenstrasse 6, D-1000 Berlin 30, Germany.

IEC 297-1 : 1986, Dimensions of mechanical structures of the 482,6 mm (19 in) series—Part 1: Panels and racks.[3]

IEC 297-3 : 1984, Dimensions of mechanical structures of the 482,6 mm (19 in) series—Part 3: Subracks and associated plug-in units.

IEC 603-2 : 1988, Connectors for frequences below 3 MHz for use with printed boards—Part 2: Two-part connectors for printed boards, for basic grid of 2,54 mm (0,1 in), with common mounting features.

IEEE Std 1101-1987, IEEE Standard for Mechanical Core Specifications for Microcomputers (ANSI).[4]

[3]IEC standards are available from the IEC Sales Department, Case Postale 131, 3 rue de Varembé, CH-1211, Genève 20, Switzerland/Suisse.

[4]IEEE publications are available from the Institute of Electrical and Electronics Engineers, Service Center, 445 Hoes Lane, P.O. Box 1331, Piscataway, NJ 08855-1331, USA.

2. Definitions

The following definitions apply to all clauses of this International Standard.

2.1 acquisition phase: The final phase of the arbitration operation entered after determining that an agent has the highest priority and the bus is available. *See:* **arbitration operation; agent.**

2.2 address transfer: The passing of address information over the multiplexed address/data bus from the bus owner in order to select the replying agent(s). *See:* **bus owner; replying agent.**

2.3 address/data bus signal group: A set of thirty-six (36) signals, consisting of 32 address/data signals and four parity signals that are used for address and data transfers.

2.4 agent: A physical unit that has an interface to the parallel system bus, for example, a single-board computer.

2.5 agent error: An agent status that indicates an error condition in a replying agent.

2.6 agent status: The condition of the replying agent, transmitted during the reply phase of a transfer operation. *See:* **reply phase; transfer operation.**

2.7 arbitration operation: The bus operation in which agents attempt to gain exclusive access to the parallel system bus.

2.8 backplane: The physical mechanism by which signals are routed between agents.

2.9 bit (b): A binary digit.

2.10 broadcast message: A sequence of one or more data transfers from the bus owner to all replying agents, with uninterrupted bus ownership.

2.11 bus clock cycle: An amount of time equal to one bus clock period, nominally 100 nanoseconds.

2.12 bus loss: The amount of time required for a valid signal transition to occur at every point on the backplane. This value is equivalent to two bus propagation delays plus the clock skew.

2.13 bus operation: The basic unit of processing whereby digital signals effect the transfer of data across an interface by means of a sequence of control signals and an integral number of bus clock cycles.

2.14 bus owner: The agent that enters the acquisition phase of the arbitration operation and initiates one or more transfer operations. *See:* **acquisition phase; arbitration operation; transfer operation.**

2.15 bus request sequence: A set of one or more arbitration operations in which all agents that simultaneously request the bus become the bus owner, one at a time. *See:* **arbitration operation; bus owner.**

2.16 byte (B): A group of eight adjacent bits operated on as a unit.

2.17 central services module (CSM): A specific module that is required in all systems using the parallel system bus. Its services, such as starting certain bus operations and guaranteeing uniform initialization of all agents, are required by all agents on the parallel system bus. It is always located in a specific slot in the system backplane. *See:* **parallel system bus.**

2.18 client: An agent that requests services of a server. *See:* **server.**

2.19 cold-start: A sequence of events performed on the application of power that ensures a uniform initialization period for all agents, giving them the ability to begin operation from a known state.

2.20 command transfer: The passing of command information over the system control signal group, from the bus owner to the replying agent(s), during the request phase of a transfer operation. Command information includes parameters for the impending transfer operation, as well as additional address space information not transmitted with the address transfer. *See:* **request phase; system control signal group.**

2.21 data transfer: The passing of data over the multiplexed address/data bus, between the bus owner and the replying agent(s), during the reply phase of a transfer operation.

2.22 driving agent: The agent that is permitted to assert or negate a signal on the bus.

2.23 dual-mode agent: An agent that supports both memory-mode and message-mode communication on the parallel system bus. *See:* **memory-mode agent; message-mode agent.**

2.24 dual-mode system: A system that supports both memory-mode and message-mode communication. A mixture of both communication types is used on the parallel system bus.

2.25 end of transfer (EOT) status: A handshake status that indicates the last data transfer of the transfer operation. *See:* **handshake status.**

2.26 exception: An abnormal condition on the bus caused by either a bus parity error, a bus time-out, a protocol violation, or a bus owner reply phase termination.

2.27 exception operation: A bus operation in which an agent places an error indication on the parallel system bus. The error indication causes all bus agents to terminate arbitration and transfer operations.

2.28 handshake status: A status transfer that indicates the exchange of data between bus owner and replying agent(s).

2.29 I/O space: The address space used for accessing peripheral devices such as communication controllers and mass storage devices.

2.30 interconnect space: The address space used for board identification, system configuration, and board specific functions such as testing and diagnostics.

2.31 interconnect template: A definition of the contents of the interconnect space of an agent.

2.32 interface: A shared boundary between modules or agents of a computer system, through which information is conveyed.

2.33 locked: A condition of the bus that guarantees exclusive access to the parallel system bus and to resources on the replying agent(s). This inhibits transfer operations between the replying agent and any other bus interface.

2.34 memory space: The address space used for accessing physical memory devices for storage and retrieval of code and data.

2.35 memory-mode agent: An agent that communicates with others by using memory and/or I/O space on the parallel system bus.

2.36 memory-mode system: A system in which the agents communicate with one another with data structures in memory and/or I/O space.

2.37 message space: The address space used for packet based communications ranging from interrupts to negotiated data movement. *See:* **packet.**

2.38 message-mode agent: An agent that exclusively uses message space for communication with other agents.

2.39 message-mode system: A system in which communication between agents is via blocks of data transmitted in the message space.

2.40 module: A basic functional unit within an agent.

2.41 nibble: A group of four adjacent bits operated on as a unit.

2.42 packet: A block of information that is transmitted within a single transfer operation in message space. *See:* **message space; transfer operation.**

2.43 parallel system bus (PSB): The signals, media and protocol used to interconnect agents in the IEEE 1296 system.

2.44 parking: The state of the bus owner where, after the completion of the current transfer operation, ownership is retained until there is a request by another agent for the use of the bus.

2.45 power failure recovery: A sequence of events that provides orderly control of system shutdown during a temporary power failure and start-up after power is restored.

2.46 protocol: The set of signaling rules used to convey information between agents.

2.47 read data transfer: One or more data transfers from a replying agent to a bus owner, with uninterrupted bus ownership.

2.48 receiver: An agent that is the recipient of the data during a solicited message. *See:* **solicited message.**

2.49 recovery phase: The final phase of an exception operation in which the parallel system bus is allowed to sit idle for a defined amount of time. *See:* **exception operation.**

2.50 reply phase: The final phase of a transfer operation that consists of one or more consecutive data and/or status transfers on the parallel system bus.

2.51 replying agent: An agent that participates in a transfer operation with the bus owner.

2.52 request phase: The initial phase of a transfer operation in which the bus owner places command and address information on the parallel system bus.

2.53 requesting agent: An agent that has entered arbitration for bus access. *See:* **arbitration operation.**

2.54 resolution phase: The initial phase of an arbitration operation in which all agents requesting access to the bus drive an arbitration ID onto the parallel system bus. Agents mutually resolve requests and allow the agent with the highest priority to gain access to the bus. *See:* **arbitration operation.**

2.55 sender: The agent that supplies the data for a solicited message. *See:* **solicited message.**

2.56 sequential transfer: A transfer operation with multiple data transfers during the reply phase. *See:* **reply phase; transfer operation.**

2.57 server: An agent that performs a service for clients. *See:* **client.**

2.58 signal phase: The initial phase of an exception operation in which all agents are notified of an error condition. *See:* **exception operation.**