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Semiconductor devices – Mechanical and climatic test methods – Part 28: Electrostatic discharge (ESD) sensitivity testing – Charged device model (CDM) – device level

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CONTENTS

FOREWORD ... 5
INTRODUCTION ... 7
1 Scope ... 8
2 Normative references ... 8
3 Terms and definitions ... 8
4 Required equipment ... 9
4.1 CDM ESD tester ... 9
4.1.1 General ... 9
4.1.2 Current-sensing element ... 10
4.1.3 Ground plane ... 10
4.1.4 Field plate/field plate dielectric layer ... 10
4.1.5 Charging resistor ... 11
4.2 Waveform measurement equipment ... 11
4.2.1 General ... 11
4.2.2 Cable assemblies ... 11
4.2.3 Equipment for high-bandwidth waveform measurement ... 11
4.2.4 Equipment for 1,0 GHz waveform measurement ... 11
4.3 Verification modules (metal discs) ... 11
4.4 Capacitance meter ... 11
4.5 Ohmmeter ... 12
5 Periodic tester qualification, waveform records, and waveform verification requirements ... 12
5.1 Overview of required CDM tester evaluations ... 12
5.2 Waveform capture hardware ... 12
5.3 Waveform capture setup ... 12
5.4 Waveform capture procedure ... 12
5.5 CDM tester qualification/requalification procedure ... 13
5.5.1 CDM tester qualification/requalification procedure ... 13
5.5.2 Conditions requiring CDM tester qualification/requalification ... 13
5.5.3 1 GHz oscilloscope correlation with high bandwidth oscilloscope ... 14
5.6 CDM tester quarterly and routine waveform verification procedure ... 14
5.6.1 Quarterly waveform verification procedure ... 14
5.6.2 Routine waveform verification procedure ... 14
5.7 Waveform characteristics ... 14
5.8 Documentation ... 16
5.9 Procedure for evaluating full CDM tester charging of a device ... 16
6 CDM ESD testing requirements and procedures ... 17
6.1 Device handling ... 17
6.2 Test requirements ... 17
6.2.1 Test temperature and humidity ... 17
6.2.2 Device test ... 17
6.3 Test procedures ... 17
6.4 CDM test recording / reporting guidelines ... 18
7 CDM classification criteria ... 18
Annex A (normative) Verification module (metal disc) specifications and cleaning guidelines for verification modules and testers ... 19

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IEC 60749-28:2017
https://standards.iteh.ai/catalog/standards/sist/0c798383-0d42-4008-933f-22742b9d820e/iec-60749-28-2017

A.1 Tester verification modules and field plate dielectric 19
A.2 Care of verification modules.. 19
Annex B (normative) Capacitance measurement of verification modules (metal discs) sitting on a tester field plate dielectric 20
Annex C (informative) CDM test hardware and metrology improvements 21
Annex D (informative) CDM tester electrical schematic 23
Annex E (informative) Sample oscilloscope setup and waveform 24
E.1 General.. 24
E.2 Settings for the 1 GHz bandwidth oscilloscope 24
E.3 Settings for the high-bandwidth oscilloscope 24
E.4 Setup 24
E.5 Sample waveforms from a 1 GHz oscilloscope 24
E.6 Sample waveforms from an 8 GHz oscilloscope 25
Annex F (informative) Field-induced CDM tester discharge procedures 27
F.1 General.. 27
F.2 Single discharge procedure.. 27
F.3 Dual discharge procedure 27
Annex G (informative) Waveform verification procedures 29
G.1 Factor/offset adjustment method 29
G.2 Software voltage adjustment method.. 32
G.3 Example parameter recording tables 34
Annex H (informative) Determining the appropriate charge delay for full charging of a large module or device 36
H.1 General.. 36
H.2 Procedure for charge delay determination.. 36
Annex I (informative) Electrostatic discharge (ESD) sensitivity testing direct contact charged device model (DC-CDM) 38
I.1 General.. 38
I.2 Standard test module 38
I.3 Test equipment (CDM simulator) 38
I.3.1 Test equipment design 38
I.3.2 DUT (device under test) support 38
I.3.3 Metal bar/board 39
I.3.4 Equipment setup 39
I.4 Verification of test equipment 39
I.4.1 General description of verification test equipment 39
I.4.2 Instruments for measurement 41
I.4.3 Verification of test equipment, using a current probe 41
I.5 Test procedure 42
I.5.1 Initial measurement 42
I.5.2 Tests 42
I.5.3 Intermediate and final measurement 43
I.6 Failure criteria 43
I.7 Classification criteria 43
I.8 Summary 43
Bibliography 44

Figure 1 – Simplified CDM tester hardware schematic 10

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IEC 60749-28:2017
https://standards.iteh.ai/catalog/standards/sist/0c798383-0d42-4008-933f-22742b9d820e/iec-60749-28-2017

Figure 2 – CDM characteristic waveform and parameters 16
Figure D.1 – Simplified CDM tester electrical schematic 23
Figure E.1 – 1 GHz TC 500, small verification module 25
Figure E.2 – 1 GHz TC 500, large verification module 25
Figure E.3 – 8 GHz TC 500, small verification module (oscilloscope adjusts for attenuation) 26
Figure E.4 – GHz TC 500, large verification module (oscilloscope adjusts for attenuation) 26
Figure F.1 – Single discharge procedure (field charging, I_{CDM} Pulse, and slow discharge)....27
Figure F.2 – Dual discharge procedure (field charging, 1st I_{CDM} pulse, no field, 2nd I_{CDM} pulse) 28
Figure G.1 – An example of a waveform verification flow for qualification and quarterly checks using the factor/offset adjustment method 30
Figure G.2 – An example of a waveform verification flow for the routine checks using the factor/offset adjustment method 31
Figure G.3 – Example of average I_{peak} for the large verification module – high bandwidth oscilloscope 32
Figure G.4 – An example of a waveform verification flow for qualification and quarterly checks using the software voltage adjustment method 33
Figure G.5 – An example of a waveform verification flow for the routine checks using the software voltage adjustment method 34
Figure H.1 – An example characterization of charge delay vs. I_p 37
Figure I.1 – Examples of discharge circuit where the discharge is caused by closing the switch 39
Figure I.2 – Verification test equipment for measuring the discharge current flowing to the metal bar/board from the standard test module 40
Figure I.3 – Current waveform....40
Figure I.4 – Measurement circuit for verification method using a current probe 41

Table 1 – CDM waveform characteristics for a 1 GHz bandwidth oscilloscope....15
Table 2 – CDM waveform characteristics for a high-bandwidth (≥ 6 GHz) oscilloscope....15
Table 3 – CDM ESDS device classification levels 18
Table A.1 – Specification for CDM tester verification modules (metal discs)....19
Table G.1 – Example waveform parameter recording table for the factor/offset adjustment method 35
Table G.2 – Example waveform parameter recording table for the software voltage adjustment method 35
Table I.1 – Dimensions of the standard test modules 38
Table I.2 – Specified current waveform 40
Table I.3 – Range of peak current I_{p1} for test equipment....41
Table I.4 – Specification of peak current I_{p1} for the current probe verification method 42

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IEC 60749-28:2017
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SEMICONDUCTOR DEVICES – MECHANICAL AND CLIMATIC TEST METHODS –

Part 28: Electrostatic discharge (ESD) sensitivity testing – Charged device model (CDM) – device level

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This standard is based on ESDA/JEDEC Joint Standard ANSI/ESDA/JEDEC JS-002 which resulted from the merging of JESD22-C101 and ANSI/ESD S5.3.1). It contains the essential elements from both standards. The co-operation of ANSI/ESDA/JEDEC is gratefully acknowledged.

The text of this International Standard is based on the following documents:

FDIS	Report on voting
47/2362/FDIS	47/2379/RVD

Full information on the voting for the approval of this International Standard can be found in the report on voting indicated in the above table.

This document has been drafted in accordance with the ISO/IEC Directives, Part 2.

A list of all parts in the IEC 60749 series, published under the general title *Semiconductor devices –Mechanical and climatic test methods*, can be found on the IEC website.

The committee has decided that the contents of this document will remain unchanged until the stability date indicated on the IEC website under "http://webstore.iec.ch" in the data related to the specific document. At this date, the document will be

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INTRODUCTION

The earliest electrostatic discharge (ESD) test models and standards simulate a charged object approaching a device and discharging through the device. The most common example is IEC 60749-26, the human body model (HBM). However, with the increasing use of automated device handling systems, another potentially destructive discharge mechanism, the charged device model (CDM), becomes increasingly important. In the CDM, a device itself becomes charged (e.g. by sliding on a surface (tribocharging) or by electric field induction) and is rapidly discharged (by an ESD event) as it closely approaches a conductive object. A critical feature of the CDM is the metal-metal discharge, which results in a very rapid transfer of charge through an air breakdown arc. The CDM test method also simulates metal-metal discharges arising from other similar scenarios, such as the discharging of charged metal objects to devices at different potential.

Accurately quantifying and reproducing this fast metal-metal discharge event is very difficult, if not impossible, due to the limitations of the measuring equipment and its influence on the discharge event. The CDM discharge is generally completed in a few nanoseconds, and peak currents of tens of amperes have been observed. The peak current into the device will vary considerably depending on a large number of factors, including package type and parasitics. The typical failure mechanism observed in MOS devices for the CDM model is dielectric damage, although other damage has been noted.

The CDM charge voltage sensitivity of a given device is package dependent. For example, the same integrated circuit (IC) in a small area package can be less susceptible to CDM damage at a given voltage compared to that same IC in a package of the same type with a larger area. It has been shown that CDM damage susceptibility correlates better to peak current levels than charge voltage.

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SEMICONDUCTOR DEVICES – MECHANICAL AND CLIMATIC TEST METHODS –

Part 28: Electrostatic discharge (ESD) sensitivity testing – Charged device model (CDM) – device level

1 Scope

This part of IEC 60749 establishes the procedure for testing, evaluating, and classifying devices and microcircuits according to their susceptibility (sensitivity) to damage or degradation by exposure to a defined field-induced charged device model (CDM) electrostatic discharge (ESD). All packaged semiconductor devices, thin film circuits, surface acoustic wave (SAW) devices, opto-electronic devices, hybrid integrated circuits (HICs), and multi-chip modules (MCMs) containing any of these devices are to be evaluated according to this document. To perform the tests, the devices are assembled into a package similar to that expected in the final application. This CDM document does not apply to socketed discharge model testers. This document describes the field-induced (FI) method. An alternative, the direct contact (DC) method, is described in Annex I.

The purpose of this document is to establish a test method that will replicate CDM failures and provide reliable, repeatable CDM ESD test results from tester to tester, regardless of device type. Repeatable data will allow accurate classifications and comparisons of CDM ESD sensitivity levels.

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2 Normative references

There are no normative references in this document.

3 Terms and definitions

For the purposes of this document, the following terms and definitions apply.

ISO and IEC maintain terminological databases for use in standardization at the following addresses:

- IEC Electropedia: available at http://www.electropedia.org/
- ISO Online browsing platform: available at http://www.iso.org/obp

3.1
CDM ESD
charged device model electrostatic discharge
electrostatic discharge (ESD) using the charged device model (CDM) to simulate the actual discharge event that occurs when a charged device is quickly discharged to another object at a lower electrostatic potential through a single pin or terminal

3.2
CDM ESD tester
charged device model electrostatic discharge tester
equipment that simulates the device level CDM ESD event using the non-socketed test method

Note 1 to entry: "Equipment" is referred to as "tester" in this document.

3.3
dielectric layer
thin insulator placed atop the field plate used to separate the device from the field plate

3.4
field plate
conductive plate used to elevate the potential of the device under test (DUT) by capacitive coupling

Note 1 to entry: See Figure 1.

3.5
ground plane
conductive plate used to complete the circuitry for grounding/discharging the DUT

Note 1 to entry: See Figure 1.

3.6
software voltage
user/operator-entered voltage that, when combined with the scale factor or offset, sets the actual field plate voltage on the system in order to achieve the waveform parameters

Note 1 to entry: Waveform parameters are defined in Table 1 or Table 2.

3.7
test condition
TC
tester plate voltage that meets the waveform parameter conditions

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Note 1 to entry: The waveform parameter conditions are found in a particular column of Table 1 and Table 2.

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4 Required equipment

4.1 CDM ESD tester

4.1.1 General

Figure 1 represents the hardware schematic for a CDM tester setup to conduct field-induced CDM ESD testing assuming the use of a resistive current probe. The DUT may be an actual device or it may be one of the two verification modules (metal discs) described in Annex A. The pogo pin shall be connected to the ground plane with a 1 Ω current path with a minimum bandwidth (BW) of 9 gigahertz (GHz). The 1 Ω pogo pin to ground connection of the resistive current sensor may be a parallel combination of a 1 Ω resistor between the pogo pin and the ground plane, and the 50 Ω impedance of the oscilloscope and its coaxial cable. In Figure 1, K1 is the switch between charging the field plate and grounding the field plate. The CDM ESD testers used within the context of this document shall meet the waveform characteristics specified in Figure 2, and Table 1 and Table 2, without additional passive or active devices, such as ferrites, in the probe's assembly.

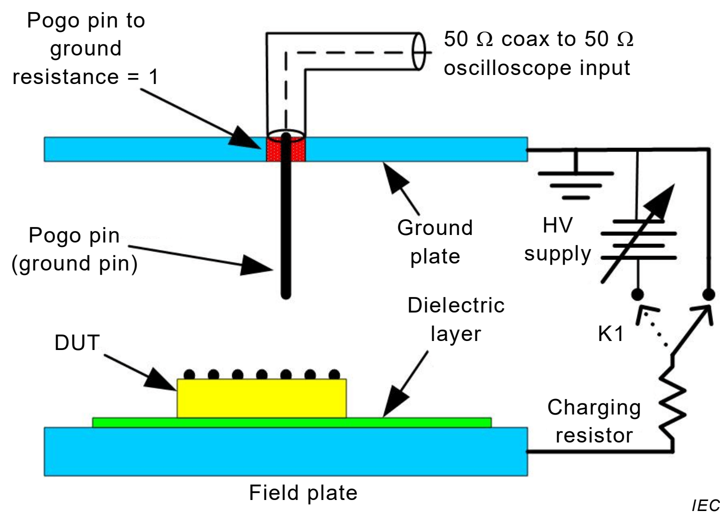

Figure 1 – Simplified CDM tester hardware schematic

When constructing the test equipment, the parasitics in the charge and discharge paths should be minimized since the resistance inductance-capacitance (RLC) parasitics in the equipment greatly influence the test results.

For existing equipment, it is recommended to contact qualified service personnel to determine compliance to this document upon removal of ferrite components.

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4.1.2 Current-sensing element

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A current-sensing element shall be incorporated into the ground plane. The resistance of this element shall have a value of (1,0 ± 10 %) Ω. A resistor, as specified in 4.1.1, shall be used as the current-sensing element. The value of resistance (including the 50 Ω cable/oscilloscope termination) shall be measured using an ohmmeter as described in 4.5. The resistance value shall be used to calculate the first peak current.

The current-sensing element shall have a minimum frequency response of 9 GHz (specified by a maximum roll-off of 3 dB at 9 GHz).

4.1.3 Ground plane

The probe assembly shall contain a square ground plane with the probe pin centred within it as shown in Figure 1. The dimensions of the ground plane shall be 63,5 mm × 63,5 mm ± 6,35 mm (2,5 inches × 2,5 inches ± 0,25 inches).

4.1.4 Field plate/field plate dielectric layer

The field plate shall have a surface flatness to vary no more than ± 0,127 mm (0,005 inches). The field plate dielectric layer should be made with an FR4 or similar epoxy-glass material. For FR4, the thickness and thickness tolerance of this dielectric layer should be 0,381 mm ± 0,0254 mm (0,015 inches ± 0,001 inches) in order to result in a capacitance measurement (as specified in normative Annex B) in the range specified in Table A.1.

If a different material is used, the material thickness is chosen to result in a capacitance measurement in the range specified in Table A.1.

4.1.5 Charging resistor

The charging resistor shown in Figure 1 shall nominally be 100 MΩ or greater.

Resistor values higher than 100 MΩ may be used, but this may not allow very large devices (refer to 5.9 and Annex H) to charge fully before being discharged by the probe assembly. This effect can be overcome by adding a delay between discharges in the CDM tester programming software. If using a resistor greater than 100 MΩ, it is recommended that the tester or the device itself be characterized to determine if a delay is needed for discharging large devices. A procedure for this large device delay characterization is given in Annex H.

4.2 Waveform measurement equipment

4.2.1 General

The CDM waveform measurement equipment shall consist of the following components.

4.2.2 Cable assemblies

Cable assemblies with combined internal tester cable and external cable total loss of no more than 2 dB at frequencies up to 9 GHz and a nominal 50 Ω impedance.

4.2.3 Equipment for high-bandwidth waveform measurement

4.2.3.1 High-bandwidth oscilloscope

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An oscilloscope or transient digitizer with a minimum real-time (single shot) 3 dB BW of at least 6 GHz and ≥ 20 gigasample/s sampling rate with a nominal 50 Ω input impedance.

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4.2.3.2 Attenuator

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A 20 dB attenuator with a precision of ±0,5 dB, at least 12 GHz BW, and an impedance of 50 Ω ± 5,0 Ω.

4.2.4 Equipment for 1,0 GHz waveform measurement

4.2.4.1 1 GHz oscilloscope

An oscilloscope or transient digitizer with a real-time (single shot) 3 dB BW of 1 GHz with a nominal 50 Ω input impedance. The sampling rate shall be ≥ 5 gigasample/s.

NOTE The user has the option of using a higher BW oscilloscope and using a hardware or software filter to produce a bandwidth and sampling rate equivalent to that specified in 4.2.4.1.

4.2.4.2 Attenuator

A 20 dB attenuator with a precision of ± 0,5 dB, at least 4 GHz BW, and an impedance of 50 Ω ± 5 Ω.

4.3 Verification modules (metal discs)

The large verification module shall have a capacitance of (55 ± 5 %) pF and the small verification module shall have a capacitance of (6,8 ± 5 %) pF. Refer to normative Annex A for information on the verification module physical dimensions and normative Annex B for information on the capacitance measurement procedure.

4.4 Capacitance meter

Capacitance meter with a resolution of 0,2 pF, a measurement accuracy of 3 %, and a measurement frequency of 1,0 MHz as described in normative Annex B.