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INTERNATIONAL STANDARD

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Electronics assembly technology –
Part 4: Endurance test methods for solder joint of area array type package surface mount devices

Technique d'assemblage des composants électroniques –
Partie 4: Méthodes d'essais d'endurance des joints brasés des composants pour montage en surface à boîtiers de type matriciel

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ELECTRONICS ASSEMBLY TECHNOLOGY –

Part 4: Endurance test methods for solder joint of area array type package surface mount devices

FOREWORD

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International Standard IEC 62137-4 has been prepared by IEC technical committee 91: Electronics assembly technology.

IEC 62137-4 (first edition) cancels and replaces IEC 62137:2004. This edition constitutes a technical revision.

IEC 62137-4 includes the following significant technical changes with respect to IEC 62137:2004:

- test conditions for use of lead-free solder are included;
- test conditions for lead-free solders are added;
- accelerations of the temperature cycling test for solder joints are added.

The text of this standard is based on the following documents:

FDIS	Report on voting
91/1188/FDIS	91/1205/RVD

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

A list of all parts in the IEC 62137 series, published under the general title *Electronics assembly technology* can be found in the IEC website.

Future standards in this series will carry the new general title as cited above. Titles of existing standards in this series will be updated at the time of the next edition.

The committee has decided that the contents of this publication will remain unchanged until the stability date indicated on the IEC web site under "http://webstore.iec.ch" in the data related to the specific publication. At this date, the publication will be

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ELECTRONICS ASSEMBLY TECHNOLOGY –

Part 4: Endurance test methods for solder joint of area array type package surface mount devices

1 Scope

This part of IEC 62137 specifies the test method for the solder joints of area array type packages mounted on the printed wiring board to evaluate solder joint durability against thermo-mechanical stress.

This part of IEC 62137 applies to the surface mounting semiconductor devices with area array type packages (FBGA, BGA, FLGA and LGA) including peripheral termination type packages (SON and QFN) that are intended to be used in industrial and consumer electrical or electronic equipment.

An acceleration factor for the degradation of the solder joints of the packages by the temperature cycling test due to the thermal stress when mounted, is described Annex A.

Annex H provides some explanations concerning various types of mechanical stress when mounted.

The test method specified in this standard is not intended to evaluate semiconductor devices themselves.

NOTE 1 Mounting conditions, printed wiring boards, soldering materials, and so on, significantly affect the result of the test specified in this standard. Therefore, the test specified in this standard is not regarded as the one to be used to guarantee the mounting reliability of the packages.

NOTE 2 The test method is not necessary, if there is no stress (mechanical or other) to solder joints in field use and handling after mounting.

2 Normative references

The following documents, in whole or in part, are normatively referenced in this document and are indispensable for its application. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60068-2-14, *Environmental testing – Part 2-14: Tests – Test N: Change of temperature*

IEC 60191-6-2, *Mechanical standardization of semiconductor devices – Part 6-2: General rules for the preparation of outline drawings of surface mounted semiconductor device packages – Design guide for 1,50 mm, 1,27 mm and 1,00 mm pitch ball and column terminal packages*

IEC 60191-6-5, *Mechanical standardization of semiconductor devices – Part 6-5: General rules for the preparation of outline drawings of surface mounted semiconductor device packages – Design guide for fine-pitch ball grid array (FBGA)*

IEC 60194, *Printed board design, manufacture and assembly – Terms and definitions*

IEC 61190-1-3, *Attachment materials for electronic assembly – Part 1-3: Requirements for electronic grade solder alloys and fluxed and non-fluxed solid solders for electronic soldering applications*

IEC 61249-2-7, *Materials for printed boards and other interconnecting structures – Part 2-7: Reinforced base materials clad and unclad – Epoxide woven E-glass laminated sheet of defined flammability (vertical burning test), copper-clad*

IEC 61249-2-8, *Materials for printed boards and other interconnecting structures – Part 2-8: Reinforced base materials clad and unclad – Modified brominated epoxide woven fibreglass reinforced laminated sheets of defined flammability (vertical burning test), copper-clad*

IEC 62137-3:2011, *Electronics assembly technology – Part 3: Selection guidance of environmental and endurance test methods for solder joints*

3 Terms definitions and abbreviations

3.1 Terms and definitions

For the purposes of this document, the terms and definitions given in IEC 60191-6-2, IEC 60191-6-5 and IEC 60194, as well as the following, apply.

3.1.1
temperature cycling life
period of time to reach a lost performance state as agreed between the trading partners during the temperature cycling test

3.1.2
momentary interruption detector
instrument capable to detect an electrical discontinuity in the daisy chain circuits

Note 1 to entry: See Annex B for the electrical continuity test of solder joint.

3.2 Abbreviations

FBGA	Fine-pitch ball grid array
BGA	Ball grid array
FLGA	Fine-pitch land grid array
LGA	Land grid array
SON	Small outline non-leaded package
QFN	Quad flat-pack non-leaded package
SMD	Surface mounting device
OSP	Organic solderability preservative
FR-4	Flame retardant type 4
FEA	Finite element method analysis
CGA	Column grid array

4 General

The regions of the solder joints to be evaluated are shown in Figure 1. The test method in this standard is applicable to evaluate the durability of the solder joints against thermal stress to the package mounted on substrate but not to test the mechanical strength of the package itself.

Therefore, the conditions for accelerated stress conditioning by a temperature cycling test may exceed the maximum allowable temperature range for the package.

The test method specified in this standard is mainly applicable to the solder joint between substrates of printed wiring board and the package as an evaluation target. However, the test results depend on conditions such as the mounting method and the condition, materials and the printed wiring board, etc. See Annex C to Annex G.

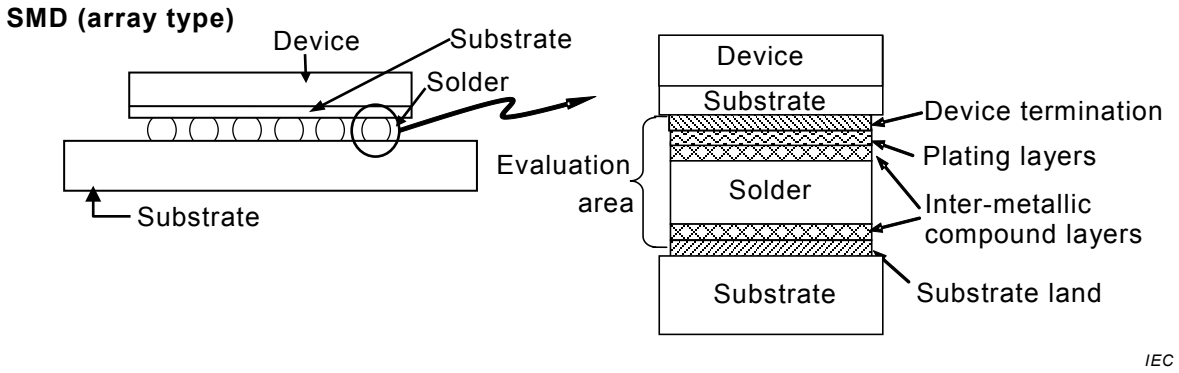


Figure 1 – Region for evaluation of the endurance test

5 Test apparatus and materials

5.1 Specimen

Specimen is the package mounted on the test substrate (refer to Clause 6 for preparation).

5.2 Reflow soldering equipment

The reflow soldering equipment shall be able to realize the reflow soldering temperature profile specified in Clause 6. Examples of temperature profile are shown in Figure 2 and Figure 3.

NOTE A standard mounting process for the package is shown in Annex G.

5.3 Temperature cycling chamber

The temperature cycling chamber shall be able to realize the temperature cycling profile specified in Figure 4. The general requirements for the temperature cycling chamber are specified in IEC 60068-2-14.

5.4 Electrical resistance recorder

The electrical resistance recorder shall be able to detect electrical continuity interruption in the daisy chain circuit. If there is no doubt of the measuring result, an electrical resistance measuring instrument featured with a momentary interruption detector and/or a continuous electrical resistance data logger should be used.

The interruption detector should be sufficiently sensitive to detect a 100 μs momentary interruption. Furthermore, the electrical resistance measuring instrument should be able to measure a resistance exceeding 1 000 Ω.

5.5 Test substrate

Unless otherwise specified in the product specification, the test substrate shall be as follows.

a) Test substrate material

Test substrate material shall be a single sided printed wiring board for general use, for example, copper-clad epoxide woven fiberglass reinforced laminated sheets as specified in IEC 61249-2-7 or IEC 61249-2-8. The thickness shall be (1,6 ± 0,2) mm including copper foil. The copper foil thickness shall be (35 ± 10) μm.

NOTE 1 Heat resistance to reflow soldering for the test substrate is described in Annex E.

b) Test substrate dimensions

The test substrate dimensions depend on the mounted package size and shape. However, the test substrate dimensions shall be fixed on the pull strength test equipment.

c) Land shape and land dimensions

Land shape and land dimensions should be as specified in IEC 61188-5-8 or as recommended by the package manufacturer.

Moreover, the test substrate and the test package shall be designed in such a way that their land pattern forms a daisy chain circuit after mounting for the electrical continuity measurement.

NOTE 2 Annex D provides a test substrate design guide.

NOTE 3 Annex C provides a solderability test for the substrate land. And Annex F provides a strength test for the substrate land.

d) Surface finish of land pattern

If specified in the product specification, a solderable region (land pattern of the test substrate) shall be treated suitably against oxidization, for example, by means of an organic solderability preservative (OSP) layer. The surface protection shall not interfere with the solderability of the land pattern being soldered by using the reflow soldering equipment specified in 5.2.

5.6 Solder paste

Solder paste is made of flux, finely divided particles of solder and additives to promote wetting and to control viscosity, tackiness, slumping, drying rate, etc. Unless otherwise specified in the product specification, one of the solder alloys listed below (as specified in IEC 61190-1-3) shall be used. The product specification shall specify details of the solder paste.

The major composition of the solder alloys are as follows:

a) 63 % mass fraction of Sn (tin) and 37 % mass fraction on Pb (lead);

b) from 3,0 % to 4,0 % mass fraction of Ag (silver), from 0,5 % to 1,0 % mass fraction of Cu (copper) and the remainder of Sn (tin).

Example: Sn-Ag-Cu ternary alloy such as Sn96,5Ag3Cu,5 alloy is used.

6 Specimen preparation

The package shall be mounted on the test substrate using the following reflow soldering process. The package for the specimen shall be modified as for test dummy package to form a daisy chain circuit with a land pattern of the test substrate after reflow soldering.

NOTE The solderability test to confirm the termination of the package and the test substrate land which affects the solder joint strength is described in Annex C.

The specimen preparation process and the conditions are as follows.

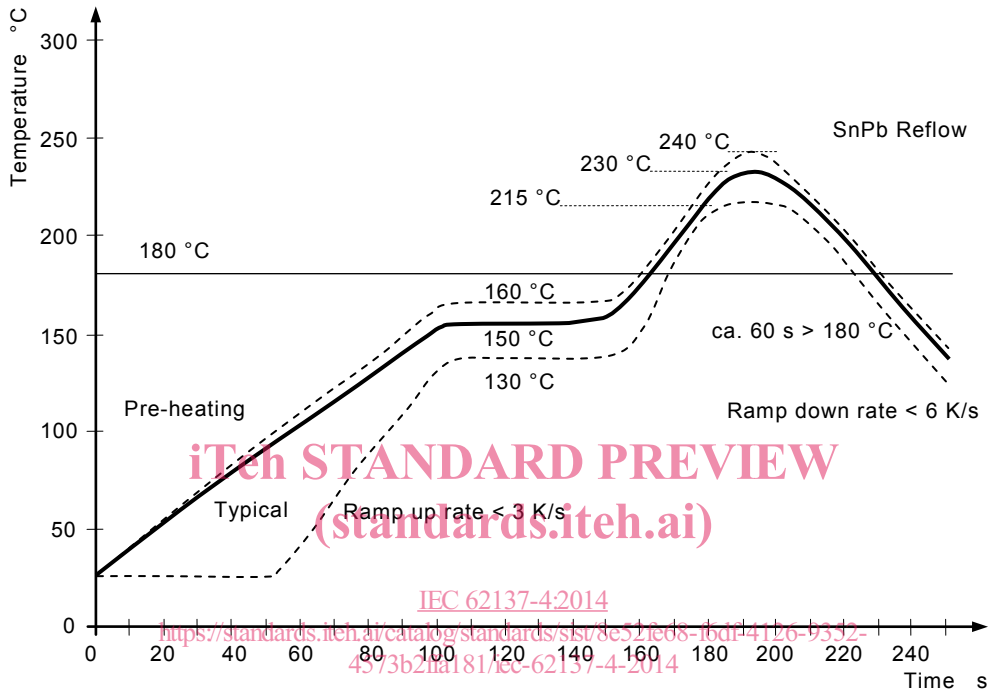
a) Unless otherwise specified in the product specification, the solder paste specified in 5.6 shall be printed on the test substrate land specified in 5.5, using a stencil made of stainless steel being 120 μm to 150 μm thick, and that have the same aperture dimensions as the dimensions, shape and arrangement of the test substrate land.

b) The package shall be placed onto the printed solder paste.

c) The reflow soldering equipment specified in 5.2 shall be used for soldering the package terminals under the conditions shown in Figure 2 or Figure 3. The measuring point of the temperature shall be on the land portion.

Figure 2 shows an example of a typical reflow soldering profile using Sn63Pb37 solder alloy, as stated in IEC 61760-1:2006, Figure 13.

Figure 3 shows an example of a typical reflow soldering profile using Sn96,5Ag3Cu,5 solder alloy, as stated in IEC 61760-1:2006, Figure 14.



Continous line: typical process (terminal temperature)

Dotted line: process limits. Bottom process limit (terminal temperature). Upper process limit (top surface temperature)

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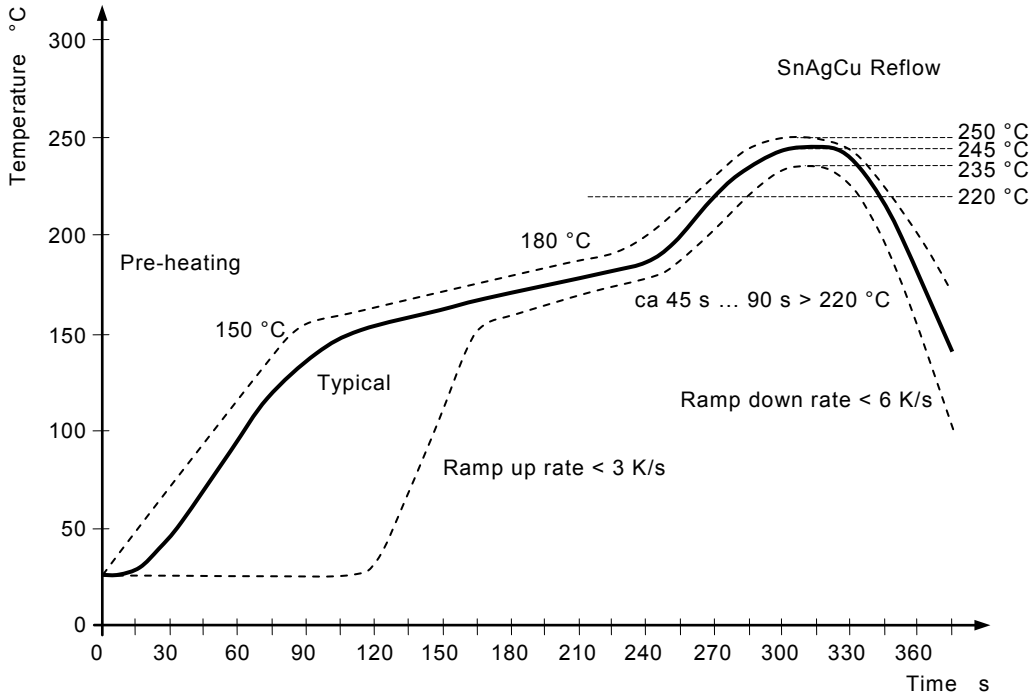
Figure 2 – Typical reflow soldering profile for Sn63Pb37 solder alloy



Continous line: typical process (terminal temperature)

Dotted line: process limits. Bottom process limit (terminal temperature). Upper process limit (top surface temperature)

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Figure 3 – Typical reflow soldering profile for Sn96,5Ag3Cu,5 solder alloy

7 Temperature cycling test

7.1 Pre-conditioning

If the specimen needs to be cleaned, the product specification should specify the cleaning method.

7.2 Initial measurement

The specimen shall be subjected to visual examination. There shall be no defect, which may impair the validity of the test.

Electrical resistance as electrical continuity of the specimen (daisy chain circuit) shall be confirmed using the momentary interruption detector specified in 5.4.

7.3 Test procedure

The temperature cycling test is according to test Na (rapid change of temperature within the prescribed time of transfer) specified in IEC 60068-2-14 with the following details.

Place the specimen in the temperature cycling chamber where the best airflow is obtained and where there is sufficient airflow around the specimen.

The test condition shall be selected from Figure 4 and Table 1, and the test shall be performed to the specified cycles in the product specification.

The electrical resistance of the daisy chain circuit shall be monitored continuously during the test using the momentary interruption detector specified in 5.4.