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Semiconductor devices – Mechanical and climatic test methods – Part 23: High temperature operating life

Dispositifs à semiconducteurs – Méthodes d'essais mécaniques et climatiques – Partie 23: Durée de vie en fonctionnement à haute température

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FOREWORD

1) The International Electrotechnical Commission (IEC) is a worldwide organization for standardization comprising all national electrotechnical committees (IEC National Committees). The object of IEC is to promote international co-operation on all questions concerning standardization in the electrical and electronic fields. To this end and in addition to other activities, IEC publishes International Standards, Technical Specifications, Technical Reports, Publicly Available Specifications (PAS) and Guides (hereafter referred to as "IEC Publication(s)"). Their preparation is entrusted to technical committees; any IEC National Committee interested in the subject dealt with may participate in this preparatory work. International, governmental and non-governmental organizations liaising with the IEC also participate in this preparation. IEC collaborates closely with the International Organization for Standardization (ISO) in accordance with conditions determined by agreement between the two organizations.
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This consolidated version of IEC 60749-23 consists of the first edition (2004) [documents 47/1735/FDIS and 47/1745/RVD] and its amendment 1 (2011) [documents 47/2017/CDV and 47/2074/RVC]. It bears the edition number 1.1.

The technical content is therefore identical to the base edition and its amendment and has been prepared for user convenience. A vertical line in the margin shows where the base publication has been modified by amendment 1. Additions and deletions are displayed in red, with deletions being struck through.

International Standard IEC 60749-23 has been prepared by IEC technical committee 47: Semiconductor devices.

This first edition is based on the IEC/PAS 62189 (2000).

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

The committee has decided that the contents of the base publication and its amendments will remain unchanged until the stability date indicated on the IEC web site under "http://webstore.iec.ch" in the data related to the specific publication. At this date, the publication will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

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SEMICONDUCTOR DEVICES – MECHANICAL AND CLIMATIC TEST METHODS –

Part 23: High temperature operating life

1 Scope

This test is used to determine the effects of bias conditions and temperature on solid state devices over time. It simulates the device operating condition in an accelerated way, and is primarily used for device qualification and reliability monitoring. A form of high temperature bias life using a short duration, popularly known as “burn-in”, may be used to screen for infant mortality related failures. The detailed use and application of burn-in is outside the scope of this standard.

2 Normative references

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60747 (all parts), *Semiconductor devices – Discrete devices and integrated circuits*

IEC 60749-34:—, *Semiconductor devices – Mechanical and climatic test methods – Part 34: Power cycling* [1]

3 Terms and definitions

For the purposes of this document, the following terms and definitions apply.

3.1
maximum operating voltage
maximum supply voltage at which a device is specified to operate in compliance with the applicable device specification or data sheet

3.2
absolute maximum rated voltage
maximum voltage that may be applied to a device, beyond which damage (latent or otherwise) may occur

NOTE It is frequently specified by device manufacturers for a specific device and/or technology.

3.3
absolute maximum rated junction temperature
maximum junction temperature of an operating device beyond which damage (latent or otherwise) may occur

NOTE 1 It is frequently specified by device manufacturers for a specific device and/or technology.

NOTE 2 Manufacturers may also specify maximum case temperatures for specific packages.

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[1] To be published.

4 Test apparatus

The performance of this test requires equipment that is capable of providing the particular stress conditions to which the test samples will be subjected.

4.1 Circuitry

The circuitry through which the samples will be biased must be designed taking into account several considerations, as outlined below.

4.1.1 Device schematic

The biasing and operating schemes shall consider the limitations of the device and shall not overstress the devices or contribute to thermal runaway.

4.1.2 Power

The test circuit shall be designed to limit power dissipation such that, if a device failure occurs, excessive power will not be applied to other devices in the sample.

4.2 Device mounting

Equipment design, if required, shall provide for mounting of devices to minimize adverse effects while parts are under stress (e.g. improper heat dissipation).

4.3 Power supplies and signal sources

Instruments (such as digital voltmeters, oscilloscopes, etc.) used to set up and monitor power supplies and signal sources shall be calibrated and have good long-term stability.

4.4 Environmental chamber

The environmental chamber shall be capable of maintaining the specified temperature within a tolerance of ±5 °C throughout the chamber while parts are loaded and unpowered.

5 Procedure

The sample devices shall be subjected to the specified or selected stress conditions for the time and temperature required.

5.1 Stress duration

The bias life duration is intended to meet or exceed an equivalent field lifetime under use conditions. The duration is established based on the acceleration of the stress. The stress duration is specified by the relevant specification. Interim measurements may be performed as necessary, subject to the restrictions in Clause 7.

5.2 Stress conditions

The stress condition shall be applied continuously (except during interim measurement periods). The time spent elevating the chamber to accelerated conditions, reducing chamber conditions to room ambient and conducting the interim measurements shall not be considered a portion of the total specified test duration.

5.2.1 Ambient temperature

Unless otherwise specified, the ambient temperature and bias for high temperature stress shall be adjusted to maintain the temperature within the desired range. Typically, a junction temperature of 125 °C for 1 000 h is used for this test. Unless otherwise specified, the ambient temperature for low temperature stress shall be a maximum of –10 °C.

5.2.2 Operating voltage

Unless otherwise specified, the operating voltage should be the maximum operating voltage specified for the device unless the conditions of 5.2.1 cannot be met. A higher voltage is permitted in order to obtain lifetime acceleration from voltage as well as temperature; this voltage shall not exceed the absolute maximum rated voltage for the device and shall be agreed upon by the device manufacturer.

5.2.3 Biasing configurations

Biasing configurations detailed below may be bias stress (static or pulsed) or operating stress (dynamic). Depending upon the biasing configuration, supply and input voltages may be grounded or raised to a maximum potential chosen to ensure a stressing temperature not higher than the maximum-rated junction temperature. Device outputs may be unloaded or loaded, to achieve the specified output voltage level. If a device has a thermal shutdown feature, it shall not be biased in a manner that could cause the device to go into thermal shutdown.

5.2.3.1 High temperature forward bias (HTFB)

The HTFB test is configured to forward bias major power handling junctions of the device samples. The devices may be operated in either a static or a pulsed forward bias mode. Pulsed operation is used to stress the devices at, or near, maximum-rated current levels. The particular bias conditions should be determined to bias the maximum number of the solid state junctions in the device. The HTFB test is typically applied on power devices, diodes and discrete transistor devices (not typically applied to integrated circuits). The HTFB test, when applied to power devices, is complementary to IEC 60749-34.

5.2.3.2 High temperature operating life (HTOL)/Low temperature operating life (LTOL)

The HTOL/LTOL test is configured to bias the operating nodes of the device samples. The devices may be operated in a dynamic operating mode. Typically, several input parameters may be adjusted to control internal power dissipation. These include supply voltages, clock frequencies, input signals, etc. that may be operated even outside their specified values, but resulting in predictable and non-destructive behaviour of the devices under stress. The particular bias conditions should be determined to bias the maximum number of potential operating nodes in the device. The HTOL test is typically applied on logic and memory devices. The LTOL test is intended to look for failures caused by hot carriers and is typically applied on memory devices or devices with submicron device dimensions.

5.2.3.3 High temperature reverse bias (HTRB)

The HTRB test is configured to reverse bias major power handling junctions of the device samples. The devices are characteristically operated in a static operating mode at, or near, maximum rated breakdown voltage and/or current levels. The particular bias conditions should be determined to bias the maximum number of the solid state junctions in the device. The HTRB test is typically applied on power devices.

5.2.3.4 High temperature gate bias (HTGB)

The HTGB test biases gate or other oxides of the device samples. The devices are normally operated in a static mode at, or near, maximum rated oxide breakdown voltage levels. The particular bias conditions should be determined to bias the maximum number of gates in the device. The HTGB test is typically used for power devices.

6 Cool-down

Devices on high temperature stress shall be cooled to 55 °C or lower before removing the bias. Cooling under bias is not required for a given technology, if verification data is provided by the manufacturer. The interruption of bias for up to 1 min, for the purpose of moving the devices to cool-down positions separate from the chamber within which life testing was performed, shall not be considered removal of bias. All specified electrical measurements shall be completed prior to any reheating of the devices, except for interim measurements subject to the restrictions of Clause 7.

NOTE Bias refers to application of voltage to power pins.

7 Measurements

The measurements, specified in the applicable life test specification, shall be made at the beginning of the life test, at the end of each interim period and at the conclusion of the life test. Interim and final measurements may include high temperature testing. However, testing at elevated temperatures shall only be performed after completion of specified room (and lower) temperature test measurements. After interim testing, bias shall be applied to the parts before heat is applied to the chamber, or within 10 min of loading the final parts into a hot chamber. Electrical testing shall be completed as soon as possible and no later than 96 h after removal of bias from devices. If the availability of test equipment or other factors makes meeting this requirement difficult, bias shall be maintained on the devices either by extending the bias life stress or keeping the devices under bias at room temperature until this 96 h window can be met. ~~This, and the high temperature testing restrictions of this clause, need not be met if verification data for a given technology is provided.~~

~~NOTE 1 If the devices have been removed from bias and the 96 h window is not met, the stress must be resumed prior to completion of the measurements. The duration of this stress should be 24 h for any portion of each week the limit is exceeded (i.e. 24 h if the limit is exceeded by ≤168 h, 48 h if the limit is exceeded by >168 h but ≤336 h, etc.). After an interim measurement, the stress should be continued from the point of interruption.~~

If the devices have been removed from bias and the 96 hour window is exceeded, the stress shall be resumed for the duration specified in Table 1 prior to completion of the measurements. After an interim measurement, the stress shall be continued from the point of interruption. This and the high temperature testing restrictions of this clause need not be met if verification data for a given technology is provided.

NOTE ~~2~~ A shorter storage period may be needed where failure mechanisms that recover in less than 96 h are suspected.

Table 1 – Additional stress requirements for parts not tested within 96 h

	Hours by which 96 h window has been exceeded			
	>0 but ≤168	>168 but ≤336	>336 but ≤504	Other
Additional stress hours required prior to performing electrical test	24	48	72	24 h for each 168 h (week) by which the 96 h window has been exceeded

8 Failure criteria

A device is classified as a failure if it does not meet the requirements of the relevant specification. Device requirements may be found in the individual parts of IEC 60747.

9 Summary

The following details shall be specified in the applicable specification:

a) stress temperature (chamber ambient) (see 5.2);
b) stress duration (see 5.1);
c) stress mounting, if special instructions are needed (see 4.2);
d) stress condition and stress circuit schematic (see 4.1);
e) sample size and acceptance number;
f) time to complete endpoint measurements, if other than specified in Clause ~~6~~ 7;
g) operating mode (see 5.2);
h) interim read points, if required (see Clause 7);
i) maximum junction temperature during stress (see 3.3);
j) verification data if cool-down under bias is not performed (see Clause 6).