

# INTERNATIONAL STANDARD

## NORME INTERNATIONALE



**Semiconductor devices – Mechanical and climatic test methods –  
Part 26: Electrostatic discharge (ESD) sensitivity testing – Human body model  
(HBM)**

**Dispositifs à semiconducteurs – Méthodes d'essais mécaniques et climatiques –  
Partie 26: Essai de sensibilité aux décharges électrostatiques (DES) – Modèle du  
corps humain (HBM)**



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IEC Central Office  
3, rue de Varembe  
CH-1211 Geneva 20  
Switzerland

Tel.: +41 22 919 02 11  
Fax: +41 22 919 03 00  
[info@iec.ch](mailto:info@iec.ch)  
[www.iec.ch](http://www.iec.ch)

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## INTERNATIONAL ELECTROTECHNICAL COMMISSION

**SEMICONDUCTOR DEVICES –  
MECHANICAL AND CLIMATIC TEST METHODS –****Part 26: Electrostatic discharge (ESD) sensitivity testing –  
Human body model (HBM)**

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International Standard IEC 60749-26 has been prepared by IEC technical committee 47: Semiconductor devices in collaboration with technical committee 101.

This third edition cancels and replaces the second edition published in 2006. This edition constitutes a technical revision. This standard is based upon ANSI/ESDA/JEDEC JS-001-2010. It is used with permission of the copyright holders, ESD Association and JEDEC Solid state Technology Association.

NOTE ANSI/ESDA/JEDEC JS-001 resulted from the merging of JESD22-A114F and ANSI/ESD STM5.1.

This edition includes the following significant technical changes with respect to the previous edition:

- a) descriptions of oscilloscope and current transducers have been refined and updated;
- b) the HBM circuit schematic and description have been improved;

- c) the description of stress test equipment qualification and verification has been completely re-written;
- d) qualification and verification of test fixture boards has been revised;
- e) a new section on the determination of ringing in the current waveform has been added;
- f) some alternate pin combinations have been included;
- g) allowance for non-supply pins to stress to a limited number of supply pin groups (associated non-supply pins) and allowance for non-supply to non-supply (i.e., I/O to I/O) stress to be limited to a finite number of 2 pin pairs (coupled non-supply pin pairs);
- h) explicit allowance for HBM stress using 2 pin HBM testers for die only shorted supply groups.

The text of this standard is based on the following documents:

| FDIS         | Report on voting |
|--------------|------------------|
| 47/2160/FDIS | 47/2167/RVD      |

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

A list of all parts in the IEC 60749 series, published under the general title *Semiconductor devices – Mechanical and climatic test methods*, can be found on the IEC website.

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# SEMICONDUCTOR DEVICES – MECHANICAL AND CLIMATIC TEST METHODS –

## Part 26: Electrostatic discharge (ESD) sensitivity testing – Human body model (HBM)

### 1 Scope

This standard establishes the procedure for testing, evaluating, and classifying components and microcircuits according to their susceptibility (sensitivity) to damage or degradation by exposure to a defined human body model (HBM) electrostatic discharge (ESD).

The purpose (objective) of this standard is to establish a test method that will replicate HBM failures and provide reliable, repeatable HBM ESD test results from tester to tester, regardless of component type. Repeatable data will allow accurate classifications and comparisons of HBM ESD sensitivity levels.

ESD testing of semiconductor devices is selected from this test method, the machine model (MM) test method (see IEC 60749-27) or other ESD test methods in the IEC 60749 series. The HBM and MM test methods produce similar but not identical results; unless otherwise specified, this test method is the one selected.

### 2 Normative references

The following documents, in whole or in part, are normatively referenced in this document and are indispensable for its application. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60749-27, *Semiconductor devices – Mechanical and climatic test methods – Part 27: Electrostatic discharge (ESD) sensitivity testing – Machine model (MM)*

### 3 Terms and definitions

For the purposes of this document, the following terms and definitions apply.

#### 3.1

##### **associated non-supply pin**

non-supply pin (typically an I/O pin) associated with a supply pin group

Note 1 to entry: A non-supply pin is considered to be associated with a supply pin group if either:

- The current from the supply pin group (i.e., VDDIO) is required for the function of the electrical circuit(s) (I/O driver) that connect (high/low impedance) to that non-supply pin.
- A parasitic path exists between non-supply and supply pin group (e.g., open-drain type non-supply pin to a VCC supply pin group that connects to a nearby N-well guard ring).

#### 3.2

##### **component**

item such as a resistor, diode, transistor, integrated circuit or hybrid circuit



### 3.3

#### **component failure**

condition in which a tested component does not meet one or more specified static or dynamic data sheet parameters

### 3.4

#### **coupled non-supply pin pair**

two pins that have an intended direct current path (such as a pass gate or resistors, such as differential amplifier inputs, or low voltage differential signaling (LVDS) pins), including analogue and digital differential pairs and other special function pairs (e.g., D+/D-, XTALin/XTALout, RFin/RFout, TxP/TxN, RxP/RxN, CCP\_DP/CCN\_DN etc.)

### 3.5

#### **data sheet parameters**

static and dynamic component performance data supplied by the component manufacturer or supplier

### 3.6

#### **withstand voltage**

highest voltage level that does not cause device failure

Note 1 to entry: The device passes all tested lower voltages (see failure Window).

### 3.7

#### **failure window**

intermediate range of stress voltages that can induce failure in a particular device type, when the device type can pass some stress voltages both higher and lower than this range

Note 1 to entry: A component with a failure window may pass a 500 V test, fail a 1 000 V test and pass 2 000 V test. The withstand voltage of this device is 500 V.

### 3.8

#### **human body model electrostatic discharge HBM ESD**

ESD event meeting the waveform criteria specified in this standard, approximating the discharge from the fingertip of a typical human being to a grounded device

### 3.9

#### **HBM ESD tester**

HBM simulator  
equipment that applies an HBM ESD to a component

### 3.10

#### **$I_{ps}$**

peak current value determined by the current at time  $t_{max}$  on the linear extrapolation of the exponential current decay curve, based on the current waveform data over a 40 nanosecond period beginning at  $t_{max}$

SEE: Figure 2 a).

### 3.11

#### **$I_{psmax}$**

highest current value measured including the overshoot or ringing components due to internal test simulator RLC parasitics

SEE: Figure 2 a).

### 3.12

#### **no connect pin**

package interconnection that is not electrically connected to a die

EXAMPLE: Pin, bump, ball interconnection.

Note 1 to entry: There are some pins which are labelled as no connect, which are actually connected to the die and should not be classified as a no connect pin.

### 3.13 non-socketed tester

HBM simulator that makes contact to the device under test (DUT), pins (or balls, lands, bumps or die pads) with test probes rather than placing the DUT in a socket

### 3.14 non-supply pins

all pins not categorized as supply pins or no connects

Note 1 to entry: This includes pins such as input, output, offset adjusts, compensation, clocks, controls, address, data, Vref pins and VPP pins on EPROM memory. Most non-supply pins transmit or receive information such as digital or analog signals, timing, clock signals, and voltage or current reference levels.

### 3.15 package plane

low impedance metal layer built into an IC package connecting a group of bumps or pins (typically power or ground)

Note 1 to entry: There may be multiple package planes (sometimes referred to as islands) for each power and ground group.

### 3.16 pre-pulse voltage

voltage occurring at the device under test (DUT) just prior to the generation of the HBM current pulse

SEE: Clause C.2.

### 3.17 pulse generation circuit

dual polarity pulse source circuit network that produces a human body discharge current waveform

Note 1 to entry: The circuit network includes a pulse generator with its test equipment internal path up to the contact pad of the test fixture. This circuit is also referred to as dual polarity pulse source.

### 3.18 ringing

high frequency oscillation superimposed on a waveform

### 3.19 shorted non-supply pin

any non-supply pin (typically an I/O pin) that is metallically connected (typically  $< 3 \Omega$ ) on the chip or within the package to another non-supply pin (or set of non-supply pins)

### 3.20 spurious current pulses

small HBM shaped pulses that follow the main current pulse, and are typically defined as a percentage of  $I_{psmax}$

### 3.21 socketed tester

an HBM simulator that makes contact to DUT pins (or balls, lands, bumps or die pads) using a DUT socket mounted on a test fixture board

### 3.22

#### **static parameters**

parameters measured with the component in a non-operating condition

Note 1 to entry: These may include, but are not limited to, input leakage current, input breakdown voltage, output high and low voltages, output drive current, and supply current.

### 3.23

#### **step stress test hardening**

ability of a component subjected to increasing ESD voltage stresses to withstand higher stress levels than a similar component not previously stressed

EXAMPLE: A component may fail at 1 000 V if subjected to a single stress, but fail at 3 000 V if stressed incrementally from 250 V.

### 3.24

#### **supply pin**

any pin that provides current to a circuit

Note 1 to entry: Supply pins typically transmit no information (such as digital or analogue signals, timing, clock signals, and voltage or current reference levels). For the purpose of ESD testing, power and ground pins are treated as supply pins.

### 3.25

#### **test fixture board**

specialized circuit board, with one or more component sockets, which connects the DUT(s) to the HBM simulator

### 3.26

#### **$t_{\max}$**

time when  $I_{ps}$  is at its maximum value ( $I_{ps\max}$ )

SEE: Figure 2a).

### 3.27

#### **trailing current pulse**

current pulse that occurs after the HBM current pulse has decayed

SEE: Clause C.1.

Note 1 to entry: A trailing current pulse is a relatively constant current often lasting for hundreds of microseconds.

### 3.28

#### **two pin tester**

A low parasitic HBM simulator that tests DUTs in pin pairs where floating pins are not connected to the simulator thereby eliminating DUT-tester interactions from parasitic tester loading of floating pins

## 4 Apparatus and required equipment

### 4.1 Waveform verification equipment

All equipment used to evaluate the tester shall be calibrated in accordance with the manufacturer's recommendation. This includes the oscilloscope, current transducer and high voltage resistor load. Maximum time between calibrations shall be one year. Calibration shall be traceable to national or international standards.

Equipment capable of verifying the pulse waveforms defined in this standard test method includes, but is not limited to, an oscilloscope, evaluation loads and a current transducer.

## 4.2 Oscilloscope

A digital oscilloscope is recommended but analogue oscilloscopes are also permitted. In order to ensure accurate current waveform capture, the oscilloscope shall meet the following requirements:

- a) Minimum sensitivity of 100 mA per major division when used in conjunction with the current transducer specified in 4.4;
- b) Minimum bandwidth of 350 MHz;
- c) For analogue scopes, minimum writing rate of one major division per nanosecond.

## 4.3 Additional requirements for digital oscilloscopes

Where a digital oscilloscope is used the following additional requirements apply:

- a) Recommended channels: 2 or more;
- b) Minimum sampling rate:  $10^9$  samples per second;
- c) Minimum vertical resolution: 8-bit;
- d) Minimum vertical accuracy:  $\pm 2,5$  %;
- e) Minimum time base accuracy: 0,01 %;
- f) Minimum record length: 10 k points.

## 4.4 Current transducer (inductive current probe)

- a) Minimum bandwidth of 200 MHz;
- b) Peak pulse capability of 12 A;
- c) Rise time of less than 1 ns;
- d) Capable of accepting a solid conductor as specified in 4.5;
- e) Provides an output voltage per signal current as required in 4.2 (This is usually between 1 mV/mA and 5 mV/mA.);
- f) Low-frequency 3 dB point below 10 kHz (e.g., Tektronix CT2) for measurement of decay constant  $t_d$  (see 5.2.3.2, Table 1, and Note below).

NOTE Results using a current probe with a low-frequency 3 dB point of 25 kHz (e.g., Tektronix CT1) to measure decay constant  $t_d$  are acceptable if  $t_d$  is found to be between 130 ns and 165 ns.

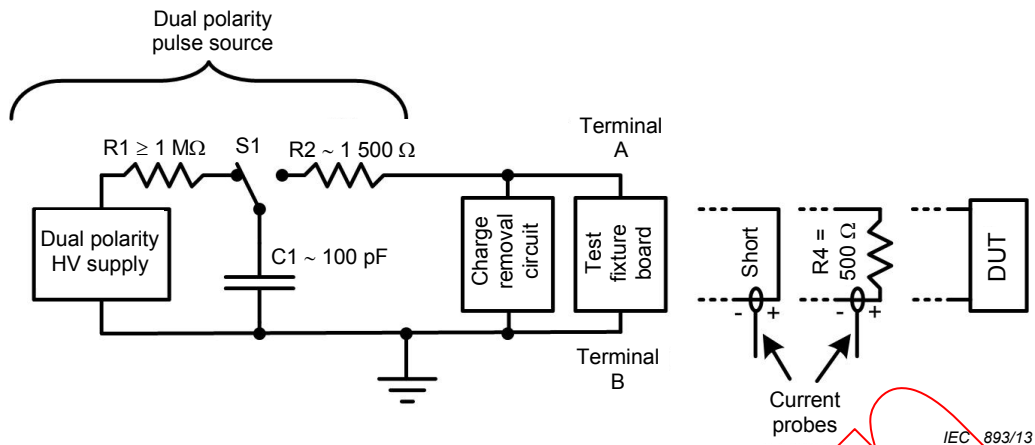
## 4.5 Evaluation loads

Two evaluation loads are necessary to verify tester functionality:

- a) Load 1: A solid 18 – 24 AWG (non-US standard wire size 0,25 to 0,75 mm<sup>2</sup> cross-section) tinned copper shorting wire as short as practicable to span the distance between the two farthest pins in the socket while passing through the current probe or long enough to pass through the current probe and contacted by the probes of the non-socketed tester.
- b) Load 2: A 500  $\Omega$ ,  $\pm 1$  %, minimum 4 000 voltage rating.

## 4.6 Human body model simulator

A simplified schematic of the HBM simulator or tester is given in Figure 1. The performance of the tester is influenced by parasitic capacitance and inductance. Thus, construction of a tester using this schematic does not guarantee that it will provide the HBM pulse required for this standard. The waveform capture procedures and requirements described in Clause 5 determine the acceptability of the equipment for use.



**Figure 1 – Simplified HBM simulator circuit with loads**

The charge removal circuit shown in Figure 1 ensures a slow discharge of the device, thus avoiding the possibility of a charged device model discharge. A simple example is a 10 kΩ or larger resistor (possibly in series with a switch) in parallel with the test fixture board. This resistor may also be useful to control parasitic pre-pulse voltages (See Annex C). The dual polarity pulse generator (source) shall be designed to avoid recharge transients and double pulses. It should be noted that reversal of terminals A and B to achieve dual polarity performance is not permitted. Stacking of DUT socket adapters (piggybacking or insertion of secondary sockets into the main test socket) is allowed only if the secondary socket waveform meets the requirements of this standard defined in Table 1.

NOTE 1 The current transducers (probes) are specified in 4.4.

NOTE 2 The shorting wire (short) and 500 Ω resistor (R4) are evaluation loads specified in 4.5.

NOTE 3 Component values are nominal.

#### 4.7 HBM test equipment parasitic properties

Some HBM simulators have been found to falsely classify HBM sensitivity levels due to parasitic artifacts or uncontrolled voltages unintentionally built into the HBM simulators. Methods for determining if these effects are present and optional mitigation techniques are described in Annex C. Two-pin testers and non-socketed testers may have smaller parasitic capacitances and may reduce the effects of tester parasitics by contacting only the pins being stressed.

## 5 Stress test equipment qualification and routine verification

### 5.1 Overview of required HBM tester evaluations

The HBM tester and test fixture boards shall be qualified, re-qualified, and periodically verified as described in this clause. The safety precautions described in 5.8 shall be followed at all times.

### 5.2 Measurement procedures

#### 5.2.1 Reference pin pair determination

The two pins of each socket on a test fixture board which make up the reference pin pair are (1) the socket pin with the shortest wiring path of the test fixture to the pulse generation circuit (terminal B) and (2) the socket pin with the longest wiring path of the test fixture from the pulse generation circuit (terminal A) to the ESD stress socket (See Figure 1). This information is typically provided by the equipment or test fixture board manufacturer. If more than one pulse generation circuit is connected to a socket then there will be more than one reference pin pair.

It is strongly recommended that on non-positive clamp fixtures, feed through test point pads be added on these paths to allow connection of either the shorting wire or 500  $\Omega$  load resistor during waveform verification measurements. These test points should be added as close as possible to the socket(s), and if the test fixture board uses more than one pulse generator, multiple feed through test points should be added for each pulse generator's longest and shortest paths.

NOTE A positive clamp test socket is a zero insertion force (ZIF) socket with a clamping mechanism. It allows the shorting wire to be easily clamped into the socket. Examples are dual in-line package (DIP) and pin grid array (PGA) ZIF sockets.

## 5.2.2 Waveform capture with current probe

### 5.2.2.1 General

To capture a current waveform between two socket pins (usually the reference pin pair), use the shorting wire (4.5, Load 1) for the short circuit measurement or the 500  $\Omega$  resistor (4.5, Load 2) for the 500  $\Omega$  current measurement and the inductive current probe (4.4).

### 5.2.2.2 Short circuit current waveform

Attach the shorting wire between the pins to be measured. Place the current probe around the shorting wire, as close to terminal B as practical, observing the polarity shown in Figure 1. Apply an ESD stress at the voltage and polarity needed to execute the qualification, re-qualification or periodic verification being conducted.

- a) For positive clamp sockets, insert the shorting wire between the socket pins connected to terminals A and B and hold in place by closing the clamp.
- b) For non-positive clamp sockets, attach the shorting wire between the socket pins connected to terminals A and B. If it is not possible to make contact within the socket, connect the shorting wire between the reference pin pair test points or socket mounting holes, if available. The design of the socket is important as some socket types may include contact springs (coils) in their design. These springs can add more parasitic inductance to the signal path and may affect the HBM waveform. Selecting sockets that minimize the use of springs (coils) is recommended, but if this is not possible, then keeping their length as short as possible is recommended.
- c) For non-socketed testers, the shorting wire with the inductive current probe is placed on an insulating surface and the simulator terminal A and terminal B probes are placed on the ends of the wires.

### 5.2.2.3 500 $\Omega$ load current waveform

Place the current probe around the 500  $\Omega$  resistor's lead, observing the polarity as shown in Figure 1. Attach the 500  $\Omega$  resistor between the pins to be measured. The current probe shall be placed around the wire between the resistor and terminal B. Apply an ESD stress at the voltage and polarity needed to execute the qualification, re-qualification or periodic verification being conducted.

- a) For socketed testers, follow procedures according to socket type as described in 5.2.2.2.
- b) For non-socketed testers, place the test load and current probe on an insulating surface and connect the tester's probes to the ends of the test load.

## 5.2.3 Determination of waveform parameters

### 5.2.3.1 Use of waveforms

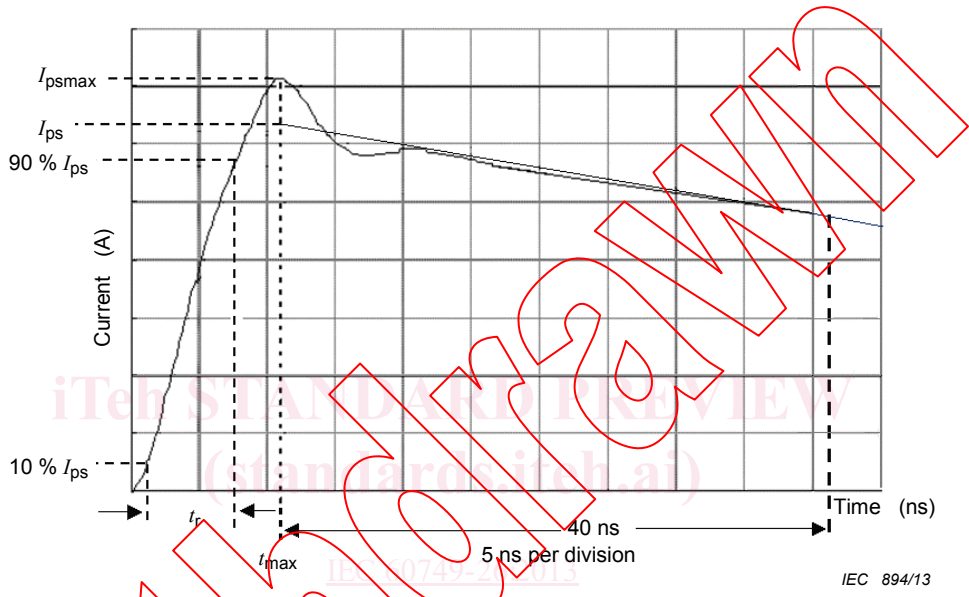
The captured waveforms are used to determine the parameter values listed in Table 1.

**5.2.3.2 Short circuit waveform**

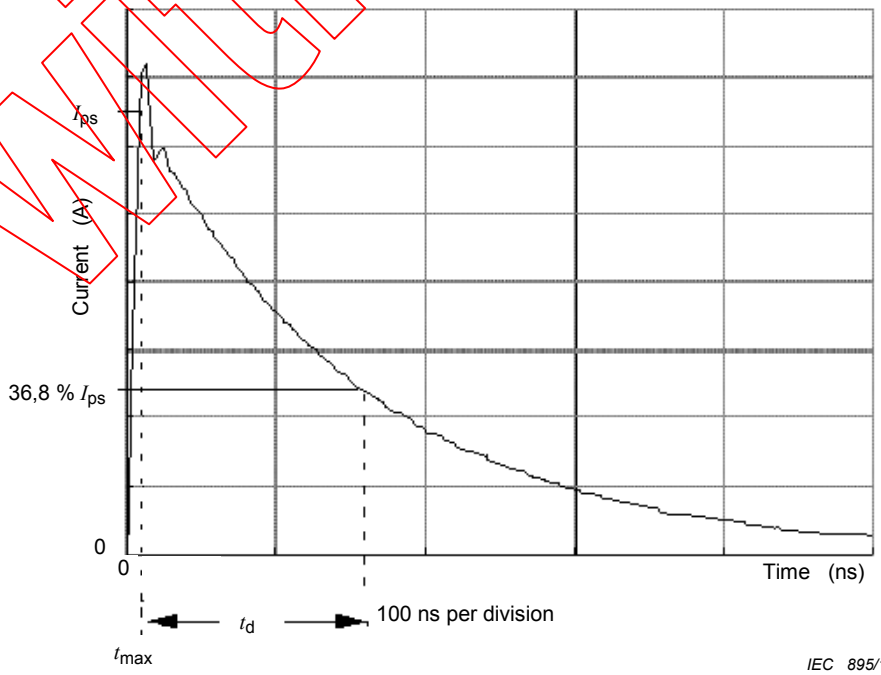
Typical short circuit waveforms are shown in Figures 2a), 2b) and 4. The parameters  $I_{ps}$  (peak current),  $t_r$  (pulse rise time),  $t_d$  (pulse decay time) and  $I_R$  (ringing) are determined from these waveforms. Ringing may prevent the simple determination of  $I_{ps}$ . A graphical technique for determining  $I_{ps}$  and  $I_R$  is described in 5.2.3.4 and Figure 4.

**5.2.3.3 500 Ω load waveform**

A typical 500 Ω load waveform is shown in Figure 3. The parameters  $I_{pr}$  (peak current with 500 Ω load) and  $t_{rr}$  (pulse rise time with 500 Ω load) are determined from this waveform.



a) Current waveform through a shorting wire ( $t_{psmax}$ )



b) Current waveform through a shorting wire ( $t_d$ )

**Figure 2 – Current waveform through shorting wires**