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Information technology – Microprocessor systems – VICbus – Inter-crate cable bus

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Foreword

ISO (the International Organization for Standardization) and IEC (the International Electrotechnical Commission) form the specialised system for world-wide standardisation. National bodies that are members of ISO or IEC participate in the development of International Standards through technical committees established by the respective organisation to deal with particular fields of technical activity. ISO and IEC technical committees collaborate in fields of mutual interest. Other international organisations, governmental and non-governmental, in liaison with ISO and IEC, also take part in the work.

In the field of information technology, ISO and IEC have established a joint technical committee, ISO/IEC JTC1. Draft International Standards adopted by the joint technical committee are circulated to national bodies for voting. Publication as an International Standard requires approval by at least 75 % of the national bodies casting a vote.

International Standard ISO/IEC 11458 was prepared by Joint technical committee ISO/IEC JTC 1, *Information technology*, SC 26: *Microprocessor Systems*.

Annex A forms an integral part of ISO/IEC 11458. Annexes B to F are for information only.

Information technology - Microprocessor systems - VICbus - Inter-crate cable bus

1 Scope

The widespread use of high-performance, multi-processor systems based on backplane buses such as the IEC 821 bus (VMEbus), has inevitably led to the requirement to create multi-crate (-subrack, -chassis, etc.) systems. The VICbus inter-crate cable bus is designed to achieve such assemblies in a standard way.

VICbus, a multiplexed, multi-master, multi-slave cable bus, connects multiple backplane buses or stand-alone devices, providing transparent, softwareless interconnection for low latency short data transactions and fast transmission of data blocks over cables of up to 100 m in length. Address and data signals, each of 32 bits, together with those necessary for the control of the bus protocols, signal multiplexing, reset and error reporting are transmitted on twisted-wire pairs using differential line drivers and receivers. Up to 31 devices are permitted on a single VICbus cable.

VICbus data transfer protocols include both a compelled mode with end-to-end acknowledgement as well as two, high speed, non-compelled modes for high rate data transfers. The compelled protocols allow both broadcast (master write) and broadcall (master read) data transfers. One of the non-compelled protocols allows broadcast transfers, whereas neither permit broadcall operation.

Inter-master arbitration uses an efficient, modified single-level, daisy-chained mechanism. The interrupt mechanism allows 32 interrupt requests, multiplexed on eight physical lines. The specification includes system failure reporting, reset and live connection and disconnection, as well as the specification of control and status registers. Particular attention has been paid to redundancy of operation.

Whilst VICbus has been derived with multi-crate backplane bus systems in mind, this specification does not preclude the design of stand-alone VICbus devices. A normative annex giving rules and recommendations for a VMEbus to VICbus interface has been included, and further, similar annexes for other backplane bus standards will be added as the need arises.

2 Introduction to the ISO/IEC 11458 VICbus standard

2.1 Objectives

VICbus is a cable bus intended to be used to connect together multiple devices, particularly backplane bus systems, efficiently and with the possibility of software transparent operation, to allow large multi-crate, multi-processor systems to be constructed.

The objectives of this standard are to:

a) provide a standard cable bus for the interconnection of multiple devices, both backplane bus systems, such as the IEC821 VMEbus, and stand-alone apparatus;

b) specify the electrical characteristics of the cable bus;

c) specify the protocols that precisely define the interaction between devices connected to the VICbus;

d) specify the mechanisms necessary to construct fault-tolerant, multi-device systems;

e) provide the necessary definitions, terminology and background information to fully describe the VICbus protocols and other mechanisms.

2.2 Standard terminology

To avoid ambiguity, and to ensure that it is clear what the requirements for compliance are, many of the paragraphs in this standard are prefixed with sequentially numbered keywords by clause (N), known collectively as **regulations**, thus:

RULE <N.n>

RECOMMENDATION <N.n>

PERMISSION <N.n>

OBSERVATION <N.n>

2.2.1 Rule <N.n>

Rules form the basis of the VICbus standard, and may be expressed in textual, diagrammatic or tabular form. They use the imperative form and include the upper case words SHALL or SHALL NOT, which are reserved for this purpose only. Rules are printed in *italics*, thus:

RULE 2.1
Example: rules contain the upper case words SHALL or SHALL NOT.

2.2.2 Recommendation <N.n>

Recommendations contain information which will be very useful, if not vital, when designing to the VICbus standard and designers are encouraged to heed the advice given to ensure the best possible interpretation of the specification's requirements.

RECOMMENDATION 2.1
Example: recommendations contain very useful information.

2.2.3 *Permission <N.n>*

Permissions clarify aspects of the standard where multiple choices might be possible, and indicate acceptable lines of approach. The upper case word MAY is reserved for this purpose only.

PERMISSION 2.1
Example: permissions help you choose and include the upper case word MAY.

2.2.4 *Observation <N.n>*

Observations serve to explain the rationale behind rules and other requirements.

OBSERVATION 2.1
Example: observations explain the rationale of certain requirements.

2.3 *Other terminology*

All normative terms (that is those having a specified meaning within the context of this document) are typed in bold font, in general the first time they appear, thus: **arbiter**. Such terms are explained in the informative glossary, included as annex B, in addition to any references within the body of the text.

2.4 *Timing diagrams*

Timing diagrams are drawn such that a high level represents the asserted state (logical 1).

2.5 *Tables*

The **asserted** (logical 1) and **deasserted** (logical 0) states are indicated in tables as "1" and "0" respectively.

2.6 *Data representation*

Table 1 shows the labelling and significance of the bytes (groups of eight bits) within the four-byte location selected by a VICbus address or by the register select signals.

Table 1 - VICbus data representation

	Most significant bit ▼			Least significant bit ▼
	Byte (0)	**Byte (1)**	**Byte (2)**	**Byte (3)**
Data bits	31.....24	23.....16	15.....8	7.....0

3 Data transfer bus

3.1 Introduction

The Data Transfer Bus (DTB) is the means by which data, address, control and status information is transferred between VICbus **devices**. The device containing the **current master** uses the address information to select one or more **participating slaves** and the addresses within them with which it wishes to exchange data. The control information specifies the direction of data transfer and the number and position of bytes within the four-byte data bus which are to be transferred.

VICbus devices can be self-contained units, interfaces between VICbus and a backplane bus such as VMEbus, or both. Thus the DTB also carries control information which indicates whether the required slave is within a participating slave device or on a backplane associated with it.

Two types of data transfer protocol are specified for use on the DTB: **compelled** and **non-compelled**. The compelled protocol uses a full handshake which permits the cycle timing to be controlled by both the master and the participating slave(s) and, if the slave is on a backplane bus, permits the VICbus timing to be interlocked with that of the backplane. The two non-compelled protocols provide a faster means of transmitting data, by eliminating the round-trip propagation time of the cable which is inherent in the compelled protocol, however they can only be used to access slaves within VICbus devices.

The VICbus arbitration mechanism (specified in clause 4) ensures that only one master may use the DTB at a time. However, the use of bus drivers with a "wired-OR" capability permits a master to transmit data to several participating slaves simultaneously (**broadcast** operation) or to receive data from several participating slaves simultaneously (**broadcall** operation) when using the compelled protocol, or when using one of the non-compelled protocols in the case of broadcast operation. Additionally, whichever protocol is in use, data transfers may be spied upon (that is read on-the-fly with no active participation in the transfer protocol by the device concerned).

The DTB consists of two groups of physical **lines**: the 42 **information lines** (AD31-AD00, CL3-CL0, ID4-ID0 and SERR) onto which logical **signals** are multiplexed, and the three **timing lines** (AS, DS and WAIT) which are not multiplexed and for which the terms "lines" and "signals" can therefore be used interchangeably.

3.2 DTB cycle types

When initiating a DTB cycle, the master transmits control information indicating the cycle type to be performed, so defining the following:

a) the data transfer protocol to be used;

b) whether the required slave is within the addressed device (**direct cycles**) or on an associated backplane bus, if the device is an interface (**transparent cycles**);

c) whether a data transfer cycle or an **interrupt acknowledge** cycle is to be performed (the latter is specified in clause 5);

d) the address width used (32 or 64 bits) on associated VMEbus backplanes;

e) the byte alignment used (VMEbus or **byte lane aligned** (BLA), specified in 3.3.12).

Table 4 details the cycle types in terms of the lines and signals used.

3.2.1 *Direct cycles*

Direct cycles access VICbus slaves within devices rather than those connected to an associated backplane bus. The RS4-RS0 signals (see 3.3.9, below), are used to select one of 32 register locations (some of which may use the A31-A02 signals for sub-addressing). The allocation of mandatory and user definable register locations is specified in clause 8.

The three direct cycle types described in this specification are listed in table 2.

RULE 3.1
A device SHALL be capable of responding to direct compelled cycles as a slave.

Table 2 - Direct cycles

Cycle type	Protocol	Data alignment	Application
Direct compelled	Compelled	Byte lane	Transfers to slaves within devices (that is not on an associated backplane bus) with handshake control
Direct non-compelled 1	Non-compelled	Byte lane	Transfers to slaves within devices with no handshake control
Direct non-compelled 2	Non-compelled	Byte lane	Transfers to slaves within devices with no immediate handshake control; the slave's responses being pipelined. The initial transfer is the exception, since it is fully handshaken in order to confirm the existence and capability of the slave

3.2.2 *Transparent cycles*

The compelled protocol is used to access slaves connected to the backplane bus associated with an interface device, and the timing is interlocked with that of the backplane bus. Note that the non-compelled protocols cannot be used to implement transparent cycles, as this interlock is not possible.

The three types of transparent cycle described in this specification are listed in table 3.

Table 3 - Transparent cycles

Cycle type	Protocol	Data alignment	Application
Transparent VME-A64 [1)]	Compelled	VMEbus	VMEbus A64 cycles are transmitted over VICbus and a corresponding A64 cycle is generated on an associated VMEbus backplane
Transparent VME	Compelled	VMEbus	VMEbus A32, A24 or A16 cycles are transmitted over VICbus and corresponding cycles are generated on an associated VMEbus backplane
Transparent BLA	Compelled	Byte lane	Cycles are generated on an associated non-VMEbus backplane (intended for future applications)

1) A64 transfers are described in the proposed revision of the VMEbus specification document known as "VME64".

3.3 *Use of the DTB information lines*

In order to keep the number of physical lines to a practical number for a cable bus, the DTB information lines are multiplexed, and a DTB cycle therefore consists of an **address phase** and a **data phase** the latter consisting of one or more data transfers. The structure of a DTB cycle is illustrated in figure 1.

3.3.1 *The address phase*

The address phase is used by the master to:

a) select the slave device or devices which it requires to participate in the cycle;

b) specify the cycle type;

c) transmit an address internal to the slave or slaves.

3.3.2 *The data phase*

The data phase is used to transmit data to and / or from the selected address within the slave or slaves. In the case of a block transfer, it transfers data to or from successive addresses.

The multiplexed signals carried by the DTB information lines during the address and data phases are shown in tables 4, 5 and 6, and defined in subclauses 3.3.3 to 3.3.15, inclusive. In some cases the signal carried by a particular line depends on the cycle type, as well as on the phase of the cycle (address or data).

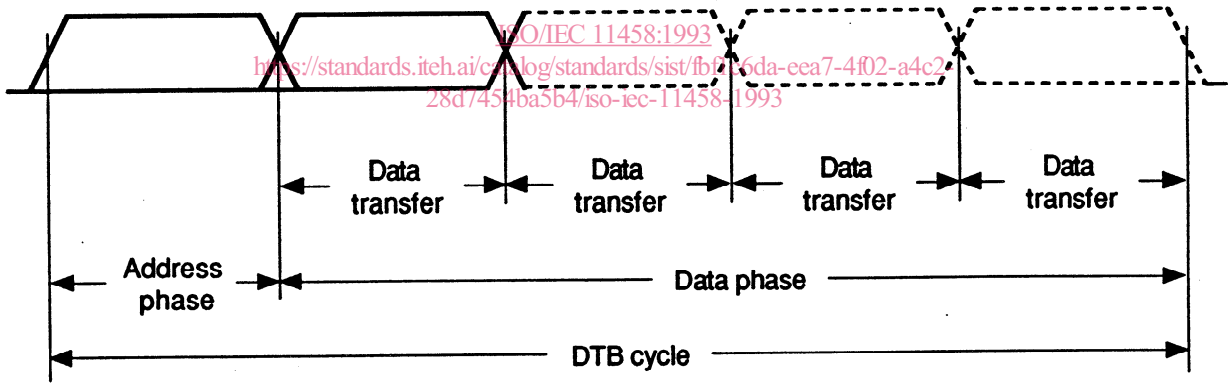

Figure 1 - DTB cycle

3.3.3 *Address / data lines AD31-AD00*

The 32 address / data lines (AD31-AD00) carry address and byte selection signals during the address phase, and data signals during the data phase.

3.3.4 *Control lines CL3-CL0*

The four control lines (CL3-CL0) carry control signals during both the address and data phases. In addition, they carry some addressing signals during the address phase of the transparent VME and VME-A64 cycle types. During the address phase, CL3 and CL2 carry cycle type definition signals, whilst CL1 and CL0 either carry further cycle type definition signals or addressing signals. During the

data phase, all four control lines carry additional protocol and byte selection signals.

3.3.5 *Identification lines ID4-ID0*

The five identification lines (ID4-ID0) carry device selection and other addressing signals. During the address phase they carry the **device number** (or, in the case of an IACK cycle, the **interrupter number**) signals. During the data phase they carry address extension signals for transparent cycles, and register select signals for direct cycles.

3.3.6 *Device number signals DN4-DN0*

The device number signals carry the highest level of addressing information. They are used by the master to select the VICbus slave device or devices which it wishes to participate in the cycle. Device numbers in the range 31-1 select individual devices, whilst device number 0 (zero) selects all on-line devices capable and willing to participate in broadcast or broadcall operations. Every slave device is normally equipped with a means (for example a switch or switches) to allow the user to set the device number by which it will be selected.

RECOMMENDATION 3.1
Equip a slave device with a means whereby a user can set the device number by which it will be selected. Design the device such that the device number can be set and is subsequently visible at its front panel.

OBSERVATION 3.1
It is the responsibility of the user to ensure that no more than one slave has a particular device number, if this is undesirable.

RULE 3.2
A cycle carrying device number 0 (zero) SHALL indicate a broadcast or broadcall cycle.

3.3.7 *Address signals A31-A02*

The address signals A31-A02 are used to select a four-byte (32 bit) location within selected slave or slaves, except during certain direct cycles when only the register select signals are used for this purpose. The selection of bytes within a four-byte location is described in 3.3.12.

PERMISSION 3.1
An interface to a backplane bus MAY provide address mapping facilities whereby the user can program the correspondence between blocks of addresses on VICbus and blocks of addresses on the backplane bus.

3.3.8 *Address extension signals AE5-AE0*

The address extension signals AE5-AE0 are used during transparent cycles to pass extra addressing information over the VICbus (for example the VMEbus address modifier signals - see annex A).

3.3.9 *Register select signals RS4-RS0*

The register select signals are used during direct cycles to select one of 32, four-byte register locations within selected slave or slaves, as specified in clause 8. For most register locations, the address signals (A31-A02) are not used and, therefore, do not need to be decoded by the slave or slaves, however, access to facilities within the device, such as banks of memory, may require their use.

Table 4 - Use of the address / data, control and identification lines

NOTE - RSVD = Reserved for future allocation. All other mnemonics are explained in the accompanying text.

Address Phase	Address / data	Control lines				Identification lines				
Cycle type	AD31-AD02[1)]	CL3	CL2	CL1	CL0	ID4	ID3	ID2	ID1	ID0
Transparent VME-A64	A31-A02	0	0	AE5	AE4	DN4	DN3	DN2	DN1	DN0
Transparent BLA	A31-A02	0	1	0	0	DN4	DN3	DN2	DN1	DN0
Reserved	A31-A02	0	1	0	1	RSVD	RSVD	RSVD	RSVD	RSVD
Reserved	A31-A02	0	1	1	0	RSVD	RSVD	RSVD	RSVD	RSVD
IACK	A31-A02	0	1	1	1	IN4	IN3	IN2	IN1	IN0
Direct compelled	A31-A02	1	0	0	0	DN4	DN3	DN2	DN1	DN0
Direct non-compelled 1	A31-A02	1	0	0	1	DN4	DN3	DN2	DN1	DN0
Direct non-compelled 2	A31-A02	1	0	1	0	DN4	DN3	DN2	DN1	DN0
Reserved	A31-A02	1	0	1	1	RSVD	RSVD	RSVD	RSVD	RSVD
Transparent VME	A31-A02	1	1	AE5	AE4	DN4	DN3	DN2	DN1	DN0

1) For details of the use of AD01 and AD00 in the address phase, see tables 5 and 6.

Data Phase	Address / data	Control lines				Identification lines				
Cycle type	AD31-AD00	CL3	CL2	CL1	CL0	ID4	ID3	ID2	ID1	ID0
Transparent VME-A64	D31-D00[2)]	BLT	WRITE	DSEL1	DSEL0	RSVD	AE3	AE2	AE1	AE0
Transparent BLA	D31-D00	BLT	WRITE	DSEL1	DSEL0	RSVD	AE3	AE2	AE1	AE0
Reserved	D31-D00	RSVD	WRITE	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD
Reserved	D31-D00	RSVD	WRITE	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD
IACK	D31-D00	RSVD	0	DSEL1	DSEL0	RSVD	RSVD	RSVD	RSVD	RSVD
Direct compelled	D31-D00	BLT	WRITE	DSEL1	DSEL0	RS4	RS3	RS2	RS1	RS0
Direct non-compelled 1	D31-D00	BLT	1	DSEL1	DSEL0	RS4	RS3	RS2	RS1	RS0
Direct non-compelled 2	D31-D00	BLT	WRITE	DSEL1	DSEL0	RS4	RS3	RS2	RS1	RS0
Reserved	D31-D00	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD
Transparent VME	D31-D00	BLT	WRITE	DSEL1	DSEL0	RSVD	AE3	AE2	AE1	AE0

2) For an explanation of the use of the AD lines in transparent VME-A64 cycles, see 3.4.