

INTERNATIONAL STANDARD

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**Semiconductor devices – Semiconductor interface for human body
communication –
Part 1: General requirements**

**Dispositifs à semiconducteurs – Interface à semiconducteurs pour les
communications via le corps humain –
Partie 1: Exigences générales**



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IEC Central Office
3, rue de Varembe
CH-1211 Geneva 20
Switzerland

Tel.: +41 22 919 02 11
Fax: +41 22 919 03 00
info@iec.ch
www.iec.ch

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SEMICONDUCTOR DEVICES –
SEMICONDUCTOR INTERFACE FOR HUMAN BODY COMMUNICATION –

Part 1: General requirements

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The text of this standard is based on the following documents:

FDIS	Report on voting
47/2267/FDIS	47/2277/RVD

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

A list of all parts in the IEC 62779 series, published under the general title *Semiconductor devices – Semiconductor interface for human body communication*, can be found on the IEC website.

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INTRODUCTION

The IEC 62779 series is composed of three parts as follow:

- IEC 62779-1 defines general requirements of a semiconductor interface for human body communication. It includes general and functional specifications of the interface.
- IEC 62779-2 defines a measurement method on electrical performances of an electrode that constructs a semiconductor interface for human body communication.
- IEC 62779-3¹ defines functional type of a semiconductor interface for human body communication, and operational conditions of the interface.

IEC 60748-4 gives requirements on interface integrated circuits for semiconductor devices. Especially, Chapter III, Section 7 in this standard is applied to interface circuits for a communication network using a general channel, such as wire or wireless. However, a channel for HBC is the human body whose channel properties, such as signal loss and delay profile, are different from the general channel, so Chapter III, Section 7 can't be applied to an interface for HBC. Furthermore, a standard on a communication protocol for body area network (BAN) – IEEE 802.15.6, which includes a communication protocol for HBC was published in 2012. A common interface for HBC should be defined to secure communication compatibility between various devices that are implemented on/inside the human body or embedded in peripheral equipments.

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¹ To be published.

SEMICONDUCTOR DEVICES – SEMICONDUCTOR INTERFACE FOR HUMAN BODY COMMUNICATION – Part 1: General requirements

1 Scope

This part of IEC 62779 defines general requirements for a semiconductor interface used in human body communication (HBC). It includes general and functional specifications of the interface, as well as limiting values and its operating conditions.

NOTE Additional information on HBC is provided in Annex A.

2 Normative references

The following documents, in whole or in part, are normatively referenced in this document and are indispensable for its application. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

None.

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3 Terms, definitions and letter symbols

For the purposes of this document, the following terms and definitions apply.

3.1 General terms

3.1.1

HBC semiconductor interface

semiconductor interface to process an electrical signal that is transmitted to the human body or received from the human body while located between the human body and HBC modem; implemented on/inside the human body and embedded in peripheral equipment

Note 1 to entry: HBC semiconductor interface consists of an electrode and analog front end. The HBC modem converts data into an electrical signal and sends it to the electrode, or receives an electrical signal from the analog front end and converts it into data.

Note 2 to entry: This note applies to the French language only.

3.1.2

electrode

physical structure to transmit an electrical signal between an analog front end and the human body while attached to or located near the human body

Note 1 to entry: An electrode transfers an electrical signal to be transmitted to a non-metallic transmission channel, the human body. It also transfers an electrical signal received from the human body to the analog front end.

3.1.3

analog front end

semiconductor integrated circuit to recover original data from a receiving signal transmitted through the human body

Note 1 to entry: Analog front end includes a powerline noise reduction filter, a signal amplifier, a high-pass filter, a comparator and a clock and data recovery (CDR) circuit to recover original data transmitted through a non-

metallic transmission channel. Also, it generates control signals to control operations of each component in the analog front end.

3.1.4

powerline noise reduction filter

circuit component in an analog front end to remove a powerline noise signal included in a receiving signal by an antenna function of the human body

Note 1 to entry: Additional information on generation of a powerline noise signal is provided in Annex B.

3.1.5

comparator

circuit component in an analog front end to compare two signals and switch its output signal to indicate which is larger

3.1.6

CDR circuit

circuit component in an analog front end to generate a clock from a receiving signal and align phase of the receiving signal to the generated clock

3.2 Rating and characteristics

3.2.1 Input characteristics

3.2.1.1

supply voltage

V_S

supply voltage to operate a HBC semiconductor interface

3.2.1.2

normal mode supply current

I_S

total supply current during normal mode of a HBC semiconductor interface

3.2.1.3

disabled mode supply current

I_{DISABLED}

total supply current during disabled mode of a HBC semiconductor interface

3.2.1.4

input impedance

Z_I

impedance seen by the human body into a HBC semiconductor interface

Note 1 to entry: Input impedance depends on input impedances of a powerline noise reduction filter, signal amplifier and high-pass filter.

Note 2 to entry: A powerline noise reduction filter removes a high-power noise signal which can saturate the active components in the interface.

3.2.2 Transfer characteristics

3.2.2.1

sensitivity level

SL

signal's minimum voltage at an input of a HBC semiconductor interface that is required to produce a signal having a specified signal-to-noise ratio at an output

Note 1 to entry: Additional information on the sensitivity level is provided in Annex C.

Note 2 to entry: This note applies to the French language only.

**3.2.2.2
dynamic range**

DR

ratio of a signal's maximum voltage at an input of a HBC semiconductor interface that can be tolerated without signal distortion to a minimum that is required to have a specific signal-to-noise ratio at an output

Note 1 to entry: Dynamic range depends on a minimum drive level of a comparator and a signal gain of a signal amplifier. Additional information on the sensitivity level is provided in Annex C.

Note 2 to entry: This note applies to the French language only.

**3.2.2.3
voltage gain**

G_V

increasing amount of a signal's voltage that is gained as passing through a signal amplifier and a high-pass filter without being attenuated or removed intentionally

**3.2.2.4
lower cut-off frequency**

f_{CUT,LOWER}

lower frequency where a receiving signal is attenuated by 3 dB as passing through a high-pass filter

**3.2.2.5
upper cut-off frequency**

f_{CUT,UPPER}

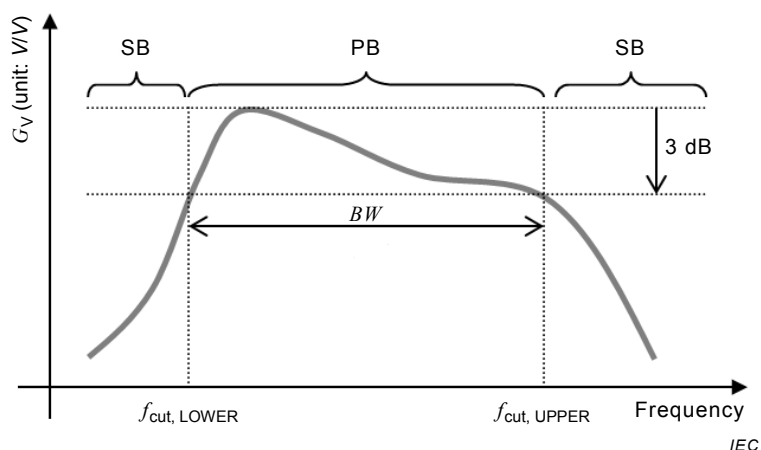
upper frequency where a receiving signal is attenuated by 3 dB as passing through a high-pass filter

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**3.2.2.6
bandwidth**

BW

frequency range width over which signals having corresponding frequencies pass through a signal amplifier and a high-pass filter without being attenuated or removed intentionally (see Figure 1)



Key

G_v	Voltage Gain	SB	Stop Band
PB	Pass Band	BW	Bandwidth
$f_{cut,LOWER}$	Upper Cut-off Frequency	$f_{cut,UPPER}$	Lower Cut-off Frequency

Figure 1 – Definition of cut-off frequency and bandwidth

Note 1 to entry: This note applies to the French language only.

3.2.2.7**lock range****LR**

frequency range's width over which the CDR circuit can be locked

Note 1 to entry: This note applies to the French language only.

3.3 Letter symbols

All the letter symbols related to input and transfer characteristics are summarized in Table 1 below.

Table 1 – Letter symbols

Name and designation	Letter symbol
supply voltage	V_S
normal mode supply current	I_S
disabled mode supply current	I_{DISABLED}
input impedance	Z_I
sensitivity level	SL
dynamic range	DR
voltage gain	G_V
lower cut-off frequency	$f_{\text{CUT,LOWER}}$
upper cut-off frequency	$f_{\text{CUT,UPPER}}$
bandwidth	BW
lock range	LR

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4 General requirements for HBC semiconductor interface**4.1 General specifications****4.1.1 General**

General specifications to specify functional and external requirements for HBC semiconductor interface shall be given.

4.1.2 Function**4.1.2.1 Category**

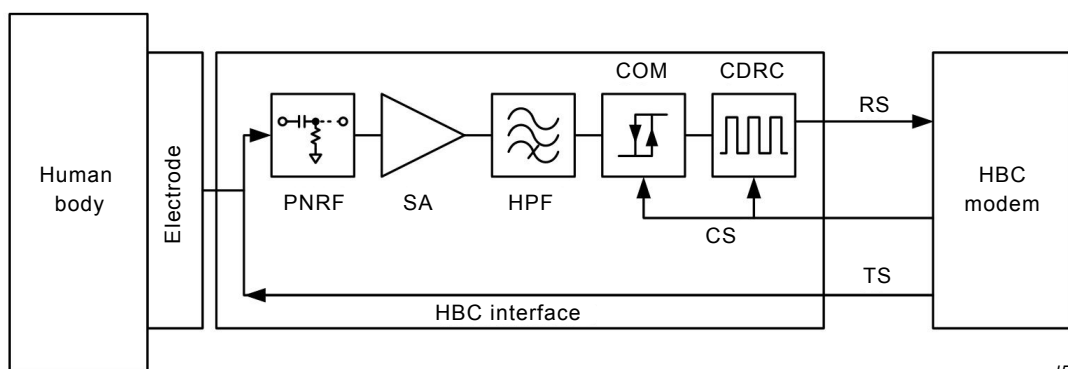
If an interface has a functional or electrical category, it shall be stated.

4.1.2.2 Functional description

A general description of the function performed by the interface shall be given.

4.1.2.3 Block diagram

The overall structure of the interface to realize the function shall be given. Details of the structure shall be given using a block diagram (see example in Figure 2).



IEC

Key

PNRF	Powerline Noise Reduction Filter	SA	Signal Amplifier
HPF	High Pass Filter	COM	Comparator
CDRC	Clock and Data Recovery Circuit	CS	Control Signal
RS	Receiving Signal	TS	Transmitting Signal

NOTE 1 The powerline noise reduction filter can be removed if the noise signal does not have enough high power to saturate the active components in the interface.

NOTE 2 The order of the components in the interface can be changed if necessary, as long as the interface satisfies the required performances.

Figure 2 – Block diagram (example)

If applicable, control signals that are transmitted between the interface and a HBC modem shall be defined in the block diagram.

4.1.3 Implementation types

4.1.3.1 Manufacturing and assembling technology

The manufacturing technologies for an electrode, for example metallic pattern, thin film, etc., and an analog front end, for example semiconductor monolithic integrated circuit, thin-film integrated circuit, hybrid integrated circuit, module, etc, shall be stated. Details of the semiconductor technologies shall be included.

An assembling technology between an electrode and an analog front end, for example modularization, integration, shall be stated.

4.1.3.2 Package technology

The package type, for example ceramic, plastic or glass, shall be given.

If applicable, the IEC and/or national reference number of the outline drawing shall be stated.

4.2 Constructional specifications

The physical specifications of an electrode, for example material, dimensions, location, shall be given.