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Edition 1.0 2015-03

TECHNICAL SPECIFICATION

SPECIFICATION TECHNIQUE

Device embedded substrate –
Part 2-1: Guidelines – General description of technology

Substrat avec appareil(s) intégré(s) –
Partie 2-1: Directives – Description générale de la technologie

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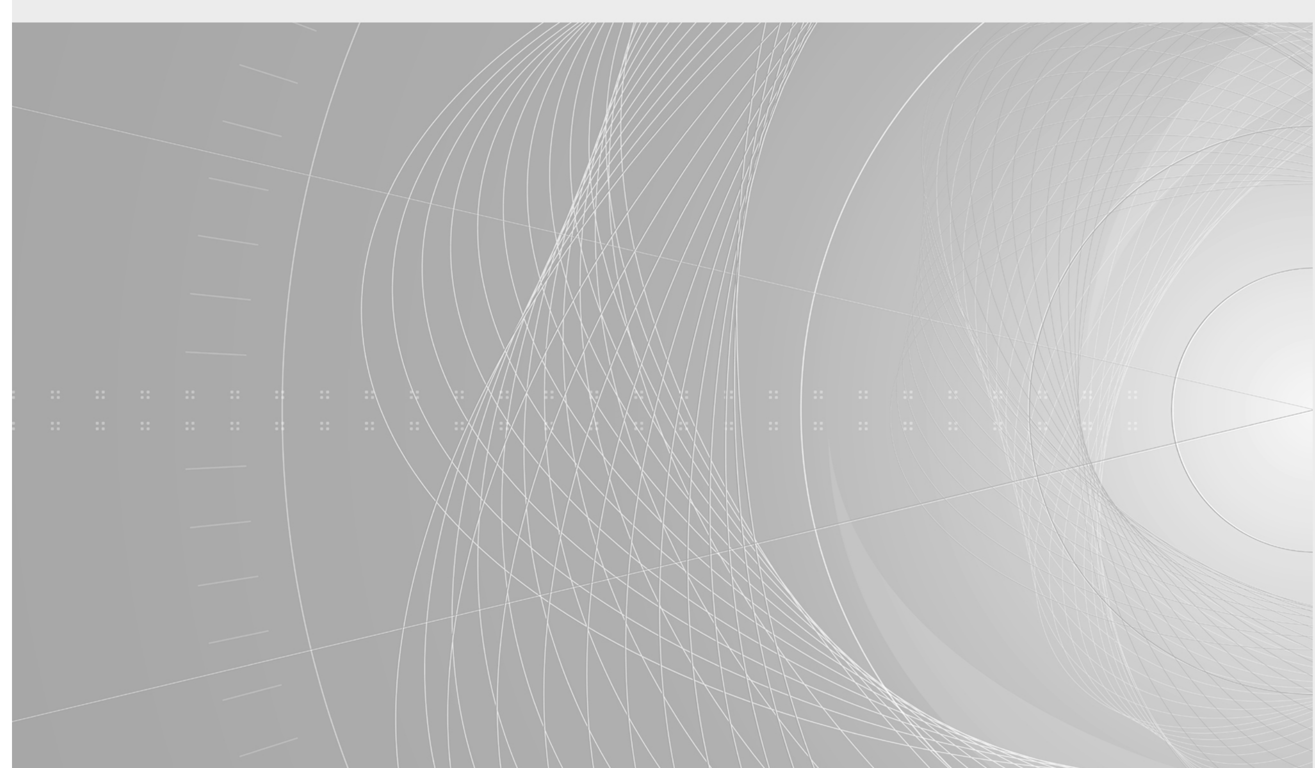

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CONTENTS

FOREWORD ... 4
INTRODUCTION ... 6
1 Scope ... 7
2 Normative references ... 7
3 Terms, definitions and abbreviations ... 7
3.1 Terms and definitions ... 7
3.2 Abbreviations ... 7
4 Technology of device embedded substrate ... 7
4.1 Basic structures ... 7
4.2 Technology of device embedded substrate ... 9
4.3 Structures of device embedded substrates and terms used in this specification ... 12
5 Jisso mounting and interconnection ... 13
5.1 General ... 13
5.2 Interconnections and structures of device embedded substrate ... 15
5.3 Device embedding by conventional process ... 17
5.4 Device embedding using vias ... 19
6 Naming of each section ... 22
6.1 General ... 22
6.2 General definition of top and bottom surfaces ... 22
6.3 Naming of layers and interconnection position ... 24
6.4 Definitions of insulation layer thickness, conductor gap and connection distance between terminal and conductor ... 27
6.4.1 General ... 27
6.4.2 Insulation layer thickness, conductor gap and electrode/conductor gap in pad connection ... 27
6.4.3 Insulation layer thickness, conductor gap and electrode/conductor gap in a via connection ... 28
6.5 Additional information ... 28
6.5.1 Additional information for the insulation layer ... 28
6.5.2 Additional information for conductor gap and electrode/conductor gap ... 29
Bibliography ... 30

Figure 1 – Examples of device embedded substrate ... 8
Figure 2 – Completed device embedded substrate (pad connection) ... 9
Figure 3 – Completed device embedded substrate (via connection) ... 9
Figure 4 – Structure of a pad connection type substrate on a passive device embedded ceramics base ... 10
Figure 5 – Structure of a device embedded substrate using a ceramic board as the base (via connection type) ... 10
Figure 6 – Entire structure of device embedded substrate ... 15
Figure 7 – Base (typical structure) ... 16
Figure 8 – Base (cavity structure) ... 16
Figure 9 – Base (insulator) ... 16

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Figure 10 – Base (Conductive carrier – metal plate) 16
Figure 11 – Passive device embedded ceramic board used as a base 17
Figure 12 – Ceramic board used as base (ceramic) 17
Figure 13 – Wire bonding connection and embedding of active device bare die 17
Figure 14 – Soldering connection and embedding of active device 18
Figure 15 – Soldering connection of square type passive device 18
Figure 16 – Conductive resin connection and embedding of active device 18
Figure 17 – Conductive resin connection and embedding of square type passive device 19
Figure 18 – Soldering connection into through hole and embedding of passive device 19
Figure 19 – Connection by copper plating after embedding of active device 19
Figure 20 – Connection by copper plating after embedding of square type passive device 20
Figure 21 – Conductive paste connection after embedding of active device package 20
Figure 22 – Conductive paste connection after embedding of square type passive device chip 20
Figure 23 – Device embedded substrate for device embedding in multi-layers 21
Figure 24 – Embedding of devices over multiple layers 21
Figure 25 – Resin base substrate 21
Figure 26 – Conductor and metal sheet/copper foil as base substrate 22
Figure 27 – Device embedded substrate using passive device embedded ceramic substrates as base substrate – Second type 22
Figure 28 – Definition of top and bottom surfaces 23
Figure 29 – Definition of top and bottom surfaces (mounting of a mother board) 23
Figure 30 – Names of layers in pad connection 24
Figure 31 – Additional information concerning the interconnection position 25
Figure 32 – Names of layers in via connection [I] 25
Figure 33 – Names of layers in via connection [II] 26
Figure 34 – Names of layers in via connection [III] 26
Figure 35 – Definition of insulating layer thickness and conductor gap in pad connection 28
Figure 36 – Definition of electrode gap in via connection 28
Figure 37 – Additional illustration of insulating layer thickness 29
Figure 38 – Additional illustration for conductor gap and electrode/connector gap 29

Table 1 – Classification of device embedding 11
Table 2 – Formed embedded device into the substrate 12
Table 3 – Embedded device structure and fabrication process 13
Table 4 – Jisso mounting and interconnection of device embedded substrate 14
Table 5 – Names of layers of device embedded board 27

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DEVICE EMBEDDED SUBSTRATE –

Part 2-1: Guidelines – General description of technology

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The text of this Technical Specification is based on the following documents:

Enquiry draft	Report on voting
91/1142/DTS	91/1163A/RVC

Full information on the voting for the approval of this Technical Specification can be found in the report on voting indicated in the above table.

A list of all parts in the IEC 62878 series, published under the general title *Device embedded substrate*, can be found on the IEC website.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

The committee has decided that the contents of this publication will remain unchanged until the stability date indicated on the IEC website under "http://webstore.iec.ch" in the data related to the specific publication. At this date, the publication will be

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INTRODUCTION

This part of IEC 62878 provides guidance with respect to device embedded substrate, fabricated by embedding discrete active and passive electronic devices into one or multiple inner layers of a substrate with electric connections by means of vias, conductor plating, conductive paste, and printing. Within the IEC 62878 series,

- IEC 62878-1-1 specifies the test methods,
- IEC TS 62878-2-1 gives a general description of the technology,
- IEC TS 62878-2-3 provides guidance on design, and
- IEC TS 62878-2-4 specifies the test element groups.

The device embedded substrate may be used as a substrate to mount SMDs to form electronic circuits, as conductor and insulator layers may be formed after embedding electronic devices.

The purpose of the IEC 62878 series is to achieve a common understanding with respect to structures, test methods, design and fabrication processes and the use of the device embedded substrate in industry.

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DEVICE EMBEDDED SUBSTRATE –
Part 2-1: Guidelines – General description of technology

1 Scope

This part of IEC 62878 describes the basics of device embedding substrate.

This part of IEC 62878 is applicable to device embedded substrates fabricated by use of organic base material, which include for example active or passive devices, discrete components formed in the fabrication process of electronic wiring board, and sheet formed components.

The IEC 62878 series neither applies to the re-distribution layer (RDL) nor to the electronic modules defined as an M-type business model in IEC 62421.

2 Normative references

The following documents, in whole or in part, are normatively referenced in this document and are indispensable for its application. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

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IEC 60194, *Printed board design, manufacture and assembly – Terms and definitions*

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IEC 61189 (all parts), *Test methods for electrical materials, printed boards and other interconnection structures and assemblies*

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3 Terms, definitions and abbreviations

3.1 Terms and definitions

For the purposes of this document, the terms and definitions given in IEC 60194 apply.

3.2 Abbreviations

BGA	ball grid array
I/O	in/out
IPD	integrated passive device
LGA	land grid array
LTCC	low temperature co-fired ceramic
MEMS	micro electro mechanical systems
PoP	package on package
QFN	quad flat no-lead package
QFP	quad flat package
SMD	surface mount device
SOJ	small outline J-leaded package
WLP	wafer level package

4 Technology of device embedded substrate

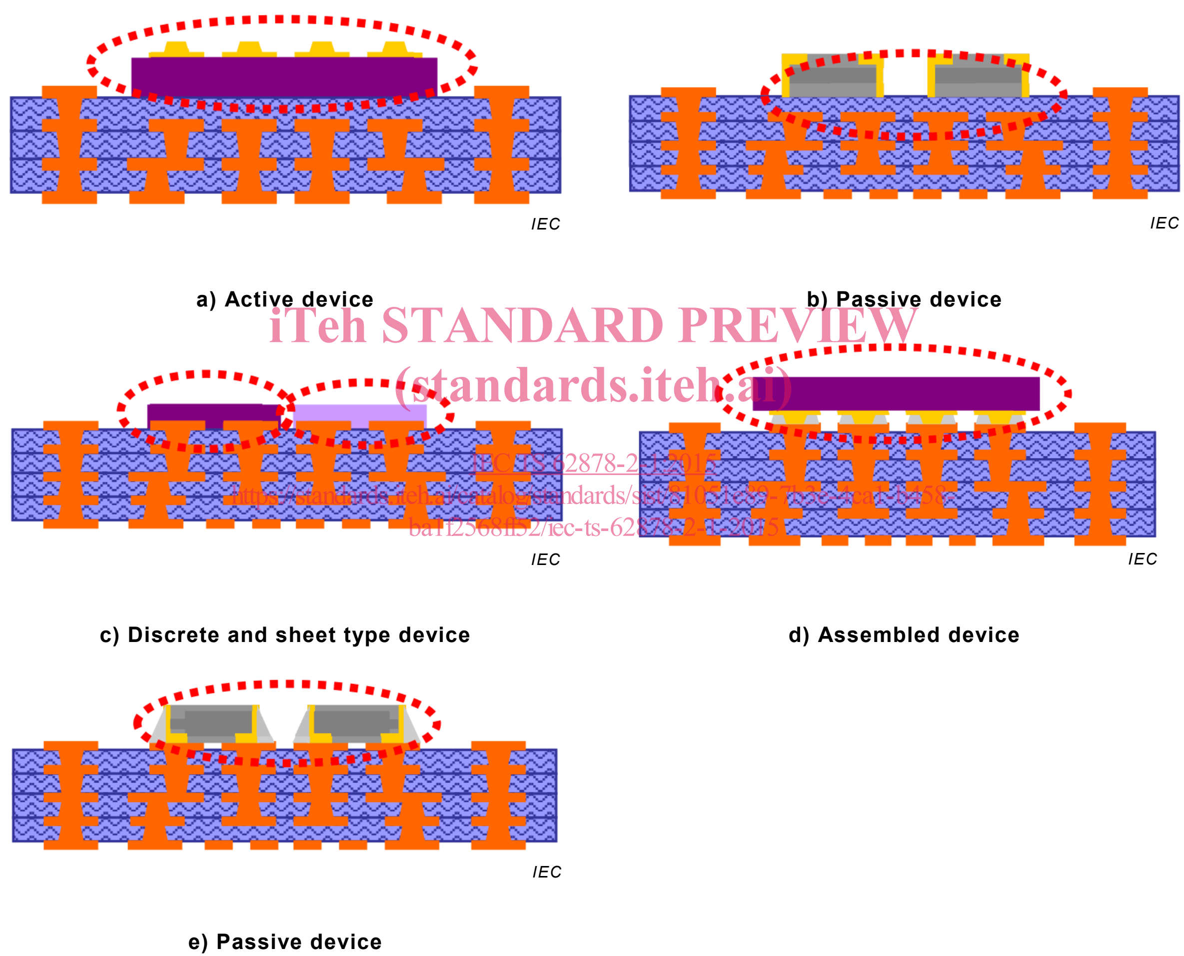
4.1 Basic structures

Figure 1 shows an example of device embedding structures in the fabrication process of a device embedded substrate. Active and passive devices are connected to each other by interlayer vias and/or conductor patterns. Insulating layers are formed using insulating materials

with vias for connection of inside conductor patterns to the conductor patterns formed on the surface(s) of the substrate. Figure 2 shows the substrate with connections using pads. Figure 3 shows the board using via connections.

The insulating layer includes rigid and flexible insulating resins such as phenol resin, epoxy resin, polyimide resin and modified polyimide resin, which may be reinforced with glass cloth, aramid cloth or paper. Interconnections include conventional interconnections to terminals of an embedded device and to a land for SMD, and formation of terminals by copper plating or vias using conductive paste.

This part of IEC 62878 does not specify a specific fabrication process of a device embedded substrate, via diameter/land diameter, conductor width/conductor spacing or a conductor line density.



a) Active device

b) Passive device

c) Discrete and sheet type device

d) Assembled device

e) Passive device

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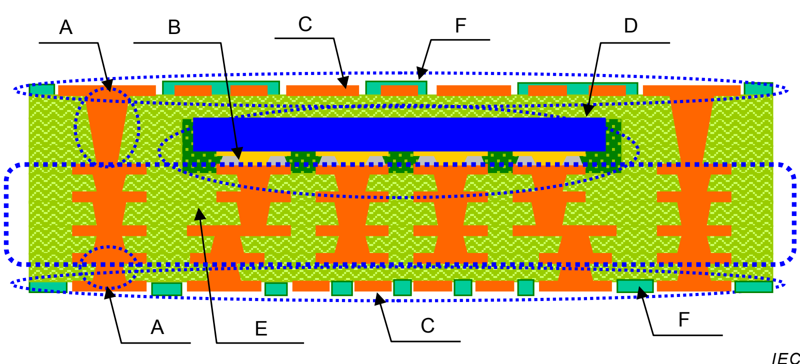
Figure 1 – Examples of device embedded substrate



Key

A	Layer connection (via)
B	Solder connection
C	Pattern formation
D	Embedded active device
E	Base
F	Solder resist

Figure 2 – Completed device embedded substrate (pad connection)

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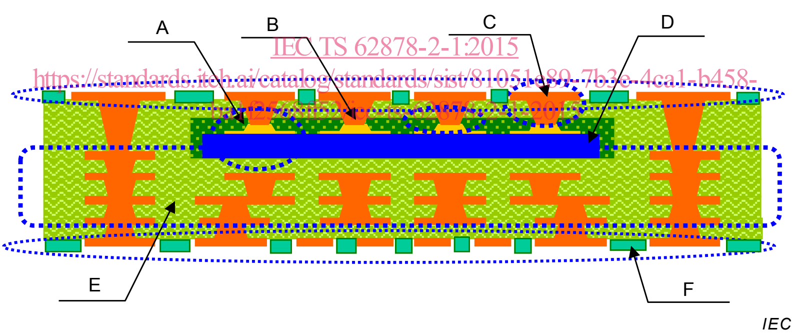


Key

A	Embedded with terminals upward
B	Copper plated connection
C	Copper plated via
D	Embedded active device
E	Base
F	Solder resist

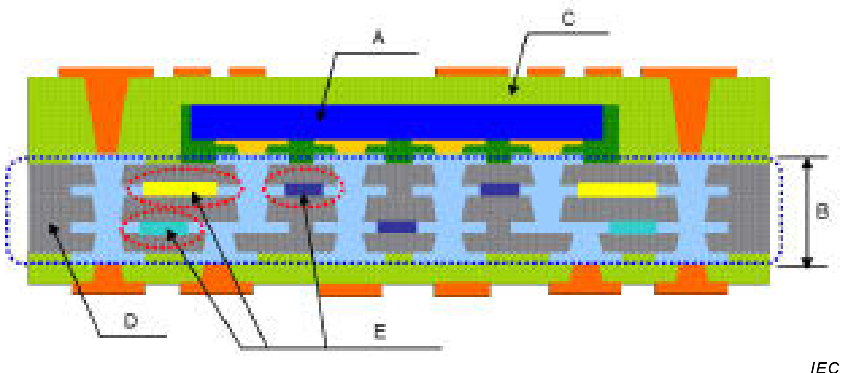
Figure 3 – Completed device embedded substrate (via connection)

4.2 Technology of device embedded substrate

There are two types of device embedded substrates. One type consists of mounting active and/or passive devices on a base substrate, then covering with organic resin; the other type consists of forming a device on a substrate and then covering it with organic resin.

Figure 4 shows the structure of a pad connection type substrate in which the active device is connected by pad onto the passive device embedded ceramics base. The device embedded substrate also includes composite type substrates which consist of mass produced inorganic

ceramics, including LTCC (low temperature co-fired ceramics, hereafter referred to as ceramics) substrates.



Key

A	Active device
B	Base
C	Embedding using resin
D	Ceramic substrate
E	Embedded devices in ceramic

Figure 4 – Structure of a pad connection type substrate on a passive device embedded ceramics base

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In the via structure type, as shown in Figure 5, the ceramic substrate is used as a base on which active and passive devices are mounted and the entire body is covered with organic resin. However, details of inorganic ceramic substrates are not specified in this part of IEC 62878. Such a ceramic substrate is treated just as a base of a device embedded substrate.

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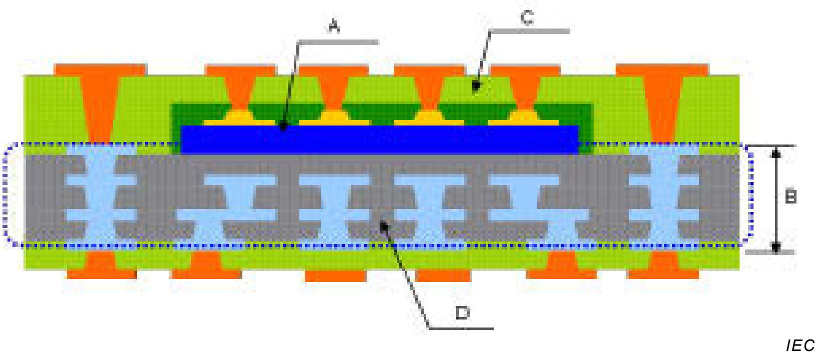

Key

A	Active device
B	Base
C	Resin embedding
D	Ceramic substrate

Figure 5 – Structure of a device embedded substrate using a ceramic board as the base (via connection type)

Classification of device embedding is given in Table 1. Active devices include for example bare die, wafer level package (WLP), ball grid array (BGA), land grid array (LGA), quad flat no lead package (QFN), small outline J-leaded package (SOJ) and quad flat package (QFP).

Passive devices include a chip component, a complex chip component like an array and an integrated passive device (IPD). Module and MEMS may be embedded into the substrate after

packaging and molding. The components formed during substrate formation are not covered by this specification and are not included in Table 2.

There are two types of embedding formed passive components. The first type consists of forming passive components using thick film or thin film technology on the base of silicon or compound semiconductor and/or on the stacked chip at the wafer level or on package-on-package (PoP). The second type consists of using a sheet-type passive device on an organic substrate followed by the embedding of other devices.

Table 1 – Classification of device embedding

Classification	Item	Embedding	Device terminals	Bonding	Schematics
Active device	Bare die	Die bonding	Peripheral	Wire bonding	
		Flip chip bonding	Peripheral area array	Flip chip bonding	
		Die bonding	Peripheral area array	Via connection (Plating, paste)	
	Wafer level package	Mounting	Peripheral area array	Soldering Conductive paste	
		Die bonding	Peripheral area array	Via connection (Plating, paste)	
	Package	Mounting	BGA, LGA, QFN	Soldering Conductive paste	
		Mounting	BGA, LGA, QFN	Via connection (Plating, paste)	
Passive device	Chip component	Mounting	Rectangular chip Rod type chip	Through hole	
		Mounting	Rectangular chip Rod type chip	Soldering Conductive paste	
		Mounting	Rectangular chip	Via connection (Plating, paste)	
	Module chip component	Mounting	Rectangular chip	Soldering Conductive paste	
		Mounting	Rectangular chip	Via connection (Plating, paste)	
	Integrated passive device	Mounting	IPD	Soldering Conductive paste	
		Mounting	IPD	Via connection (Plating, paste)	
Module	Packaging and molding	Mounting	Arbitrary	Soldering Conductive paste	

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Classification	Item	Embedding	Device terminals	Bonding	Schematics
		Mounting	Arbitrary	Via connection (Plating, paste)	
MEMS	Packaging and molding	Mounting	Arbitrary	Soldering Conductive paste	
		Mounting	Arbitrary	Via connection (Plating, paste)	

Table 2 – Formed embedded device into the substrate

Classification	Item	Embedding	Device terminals	Bonding	Schematics
Active device	Formed	Thin film sputtering	Silicon	Via connection (Plating, paste)	
		Thick film screen printing	Semiconducting polymer		
Passive device	Formed	Double through hole	Copper plating		
		Etching	Laminate material		
		Etching	Film		
		Screen printing	Polymer		
		Transfer	Ferromagnetic ceramics		
		Lamination	Seeding		
		Spin coating	Polymer		

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4.3 Structures of device embedded substrates and terms used in this specification

Structures and fabrication processes of device embedded substrates are illustrated in Table 3. A base substrate is necessary for a device embedded substrate to embed active and passive devices. Most of the base substrates are multilayer substrates and/or build-up substrates which are made of insulating resin board; insulating sheet, metal sheet and film carrier can also be used. Table 3 shows the methods to embed active or passive devices and then connect devices to the surface conductor by plated through hole vias and/or conductive paste, and checking items during the fabrication process.

This specification, however, does not cover active devices formed on silicon interposer, compound semiconductor substrates or a printed wiring board and formed passive device (resistor, capacitor or inductor). On the other hand it covers an inductor formed together with the formation of conductor pattern and the capacitor with via-in-via structure.

Table 3 – Embedded device structure and fabrication process

Process	Item	Structure		To check
		Pad bonding	Via connection	
1	Base			Opening, short-circuiting
2	Mounting			Position accuracy
3	Pad bonding		-	Connection, conduction
4	Embedding			Microvoid Board thickness Flatness
5	Via forming			Hole position Terminal position Resistance to chemicals
6	Via connection	-		Thicknesses of copper plating and conductive paste Microvoid
7	Pattern formation (multi-layer)			Open, short
8	Surface treatment (Solder mask, etc.)			Visual inspection

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5 Jisso mounting and interconnection

5.1 General

There are two types of terminal connection. One type consists of connecting the terminals of an embedded device to connecting pads formed on the base, and the other consists of forming connecting vias on the device after embedding. The device is connected to pads on the base using conventional semiconductor and SMD mounting techniques and then the device is embedded. In the second type, the device is connected to a conductor pattern after it has been embedded by copper plating or conductive paste. Both device mounting types can be classified into die-bonding and mounting methods, as shown in Table 4.