

# TECHNICAL SPECIFICATION

# SPECIFICATION TECHNIQUE



**Device embedded substrate –**  
**Part 2-4: Guidelines – Test element groups (TEG)**  
**(standards.iteh.ai)**

**Substrat avec appareil(s) intégré(s) –**  
**Partie 2-4: Directives – Groupes d'éléments d'essai (TEG)**  
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# TECHNICAL SPECIFICATION

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ICS 31.180; 31.190

ISBN 978-2-8322-2435-9

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## DEVICE EMBEDDED SUBSTRATE –

## Part 2-4: Guidelines – Test element groups (TEG)

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IEC TS 62878-2-4, which is a Technical Specification, has been prepared by IEC technical committee 91: Electronics assembly technology

The text of this Technical Specification is based on the following documents:

Enquiry draft	Report on voting
91/1144/DTS	91/1165A/RVC

Full information on the voting for the approval of this Technical Specification can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

A list of all parts in the IEC 62878 series, published under the general title *Device embedded substrate*, can be found on the IEC website.

The committee has decided that the contents of this publication will remain unchanged until the stability date indicated on the IEC website under "http://webstore.iec.ch" in the data related to the specific publication. At this date, the publication will be

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- reconfirmed,
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## INTRODUCTION

This part of IEC 62878 provides guidance with respect to device embedded substrate, fabricated by embedding discrete active and passive electronic devices into one or multiple inner layers of a substrate with electric connections by means of vias, conductor plating, conductive paste, and printing. Within the IEC 62878 series,

- IEC 62878-1-1 specifies the test methods,
- IEC TS 62878-2-1 gives a general description of the technology,
- IEC TS 62878-2-3 provides guidance on design, and
- IEC TS 62878-2-4 specifies the test element groups.

The device embedded substrate may be used as a substrate to mount SMDs to form electronic circuits, as conductor and insulator layers may be formed after embedding electronic devices.

The purpose of the IEC 62878 series is to achieve a common understanding with respect to structures, test methods, design and fabrication processes and the use of the device embedded substrate in industry.

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## DEVICE EMBEDDED SUBSTRATE

### Part 2-4: Guidelines – Test element groups (TEG)

#### 1 Scope

This part of IEC 62878 describes the test element group devices useful when measuring basic properties of device embedded substrates.

This part of IEC 62878 is applicable to device embedded substrates fabricated by use of organic base material, which include for example active or passive devices, discrete components formed in the fabrication process of electronic wiring board, and sheet formed components.

The IEC 62878 series neither applies to the re-distribution layer (RDL) nor to the electronic modules defined as an M-type business model in IEC 62421.

#### 2 Normative references

The following documents, in whole or in part, are normatively referenced in this document and are indispensable for its application. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60194, *Printed board design, manufacture and assembly – Terms and definitions*

IEC 62878-1-1, *Device embedded substrate – Part 1-1: Generic specification – Test methods*<sup>1</sup>

#### 3 Terms, definitions and abbreviations

##### 3.1 Terms and definitions

For the purposes of this document, the terms and definitions given in IEC 60194 apply.

##### 3.2 Abbreviations

AABUS	as agreed between user and supplier
AV	audiovisual
L/S	line and space
SMD	surface mount device

#### 4 Test conditions and sample preparation

##### 4.1 General

Clause 4 describes the test conditions for device embedded boards to be used in electronics equipment and reliability, and Clause 5 describes the test element group (hereafter referred to as TEG) to be used as dummy test chips, as well as test patterns used in TEGs.

##### 4.2 Test conditions

###### 4.2.1 Classification of tests and evaluation

Subclause 4.2.1 describes the classification of test levels in various applications. The environment in which products are used is divided into

<sup>1</sup> To be published.

- consumer applications (portable and non-portable), and
- industrial and automotive applications (AV/information, car operation control, and engine control).

Evaluation tests are divided into tests for package, module board and mother board. In this part of IEC 62878, “mother board” indicates the main board to which packages or modules are assembled. Three ranks are specified for evaluation levels for embedded devices (passive and active), board materials, assembly methods, and specification and characteristics of embedding devices. Evaluation levels are to be agreed between user and supplier (hereafter referred to as AABUS). Table 1 shows the above mentioned classification of user environment for each application.

**Table 1 – Application and embedded device**

Products		Package			Module			Mother board		
Applications		– Consumer (portable and non-portable) – Industrial – Automotive (audiovisual information, car operation control and engine control)								
Device	Passive	○		○	○		○	○		○
	Active	○	○		○	○		○	○	

#### 4.2.2 Measuring environment

The test environment adopted in the tests described in IEC 62878-1-1 is specified in 4.2.2. Tests are performed, unless otherwise specified, in the standard atmospheric pressure of 86 kPa to 106 kPa and air flow of smaller than 1 m/s. If it is difficult to test a specimen in the standard condition, a test may be carried out in a condition other than the standard condition when there is no question in evaluating test results. The test shall be carried out with the conditions shown in Table 2 when there is no question concerning the test result, or it shall be specifically requested by the user and supplier.

**Table 2 – Measuring environment**

Classification		Temperature °C	Humidity %	Pressure kPa	Remarks
Standard condition	Common	15 to 35	25 to 75	86 to 106	Use the standard testing condition, if not specified
	23/50	Class 1	23 ± 1	50 ± 5	
		Class 2	23 ± 2	50 ± 10	
	27/65	Class 1	27 ± 1	65 ± 5	86 to 106
Class 2		27 ± 1	65 ± 5		
Evaluation	Common	20 ± 2	60 to 70	86 to 106	

#### 4.2.3 Test methods

Test methods using TEG are as described in this part of IEC 62878. These test methods especially comprise electrical and mechanical tests. Tests for other items described in this part of IEC 62878 may be carried out AABUS.

### 4.3 Test specimens and number of specimens

#### 4.3.1 Specimen

Test specimen is either a) or b) as listed below. The surface of a specimen shall not be contaminated by grease, sweat or other foreign objects.

## a) Actual device embedded board

Cut a specimen for the test from the product of a shape and size as specified by individual specifications using a method that does not affect the performance of the specimen.

## b) Test pattern specimen

Use TEG and applicable circuit for the test of an embedded device itself. Prepare a test pattern specimen of a board and embedded device(s) using the same material as that used in the actual device embedded board. Use the same procedure to prepare a test device as for the embedded device.

**4.3.2 Number of specimens**

The number of specimens used in a test shall be either a) or b) as specified by the manufacturing status below. The agreement between user and supplier, if there is any, shall have priority.

## a) Test production

$n \geq 5$  of the unit AABUS.

## b) Volume production

$n \geq 10$  of the unit AABUS.

**4.3.3 Test report**

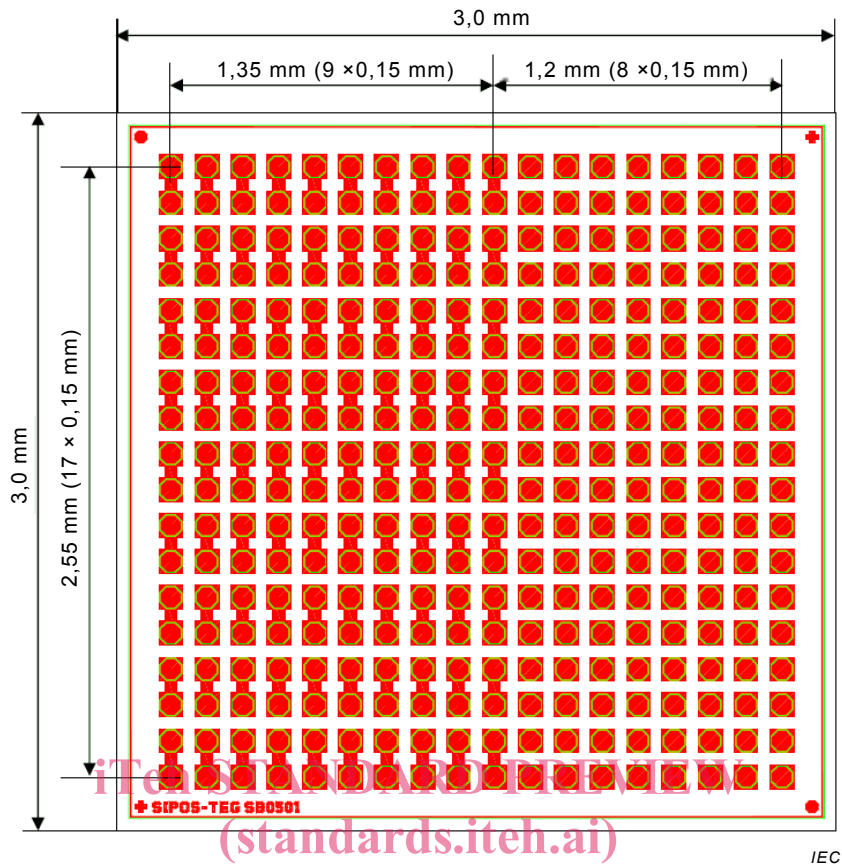
The test items shall be chosen from the list stated below AABUS, and the items shall be included in the test report:

- a) date of the test;
- b) test location;
- c) name, type and size of the embedded device;
- d) material, size and layer structure of the test board;
- e) assembly technique of the embedded device (interconnection, embedding, etc.);
- f) design specification and product specification of the test board;
- g) test equipment (specifications of the test system and equipment, jigs, material, shape, etc.);
- h) test condition (temperature, humidity, applied voltage, current, number of repetitions, time, etc.);
- i) graphs and figures showing relations between test condition and result;
- j) defect mode (photographs, etc.).

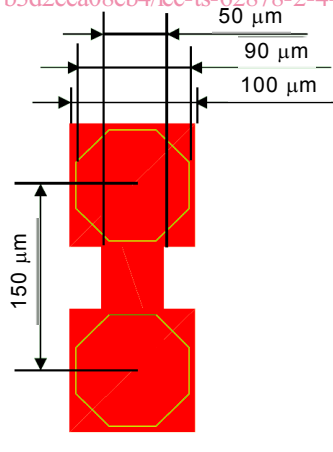
**5 TEG****5.1 Preparation of the TEG**

For the testing of device embedded substrate, TEG made up of neutral aluminium wiring is prepared. It is recommended that the passive device be replaced by a copper wiring board or that a zero ohm jumper resistor be used.

Examples of TEG are shown in Figure 1 and Figure 2. TEG-A is a sample of daisy chain to investigate connectivity. TEG-B is to measure leakage current and capacitance.



a) TEG-A – Entire view of TEG of 150 µm pitch chip  
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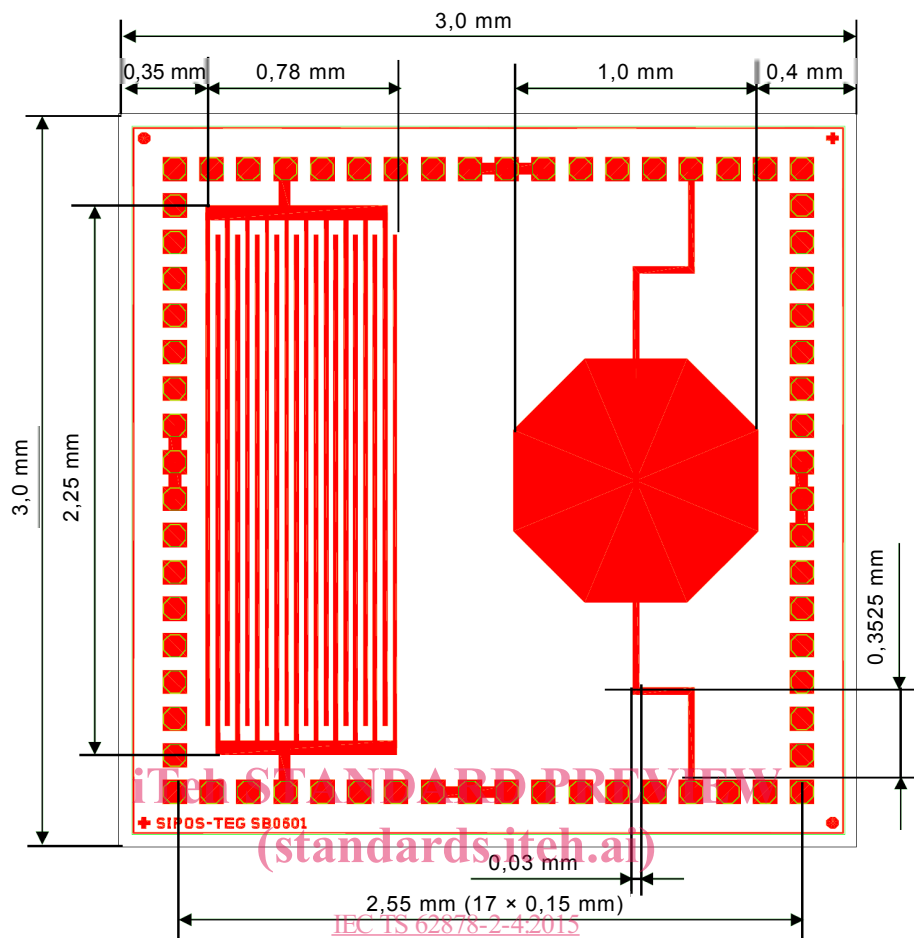


b) Detail of pad

Specification of TEG-A 150 µm pitch chip

Name: SIPOS-TEG SB0501	Distance between pad edges: 50 µm
Pad pitch: 150 µm	Chip size: 3,0 mm × 3,0 mm
Number of pads: 324 (18 × 18)	Daisy chain pad: 180
Pad size: 100 µm × 100 µm (aluminium wiring)	Independent pad: 144
Scribe width: 100 µm	Pad opening: $\varphi = 90 \mu\text{m}$ (pad opening)

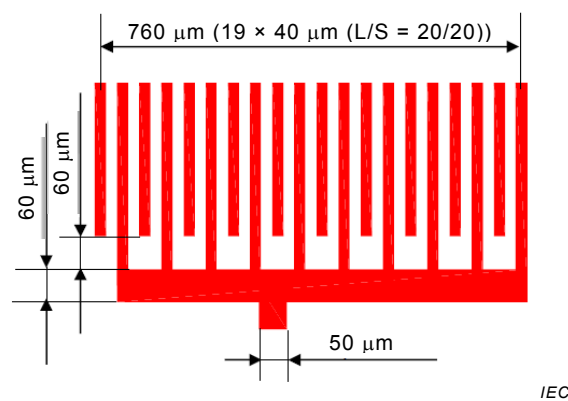
Figure 1 – Area array arrangement – TEG for conductor resistivity and via-to-via insulation



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a) TEG-B Entire view of TEG of 150 μm pitch chip



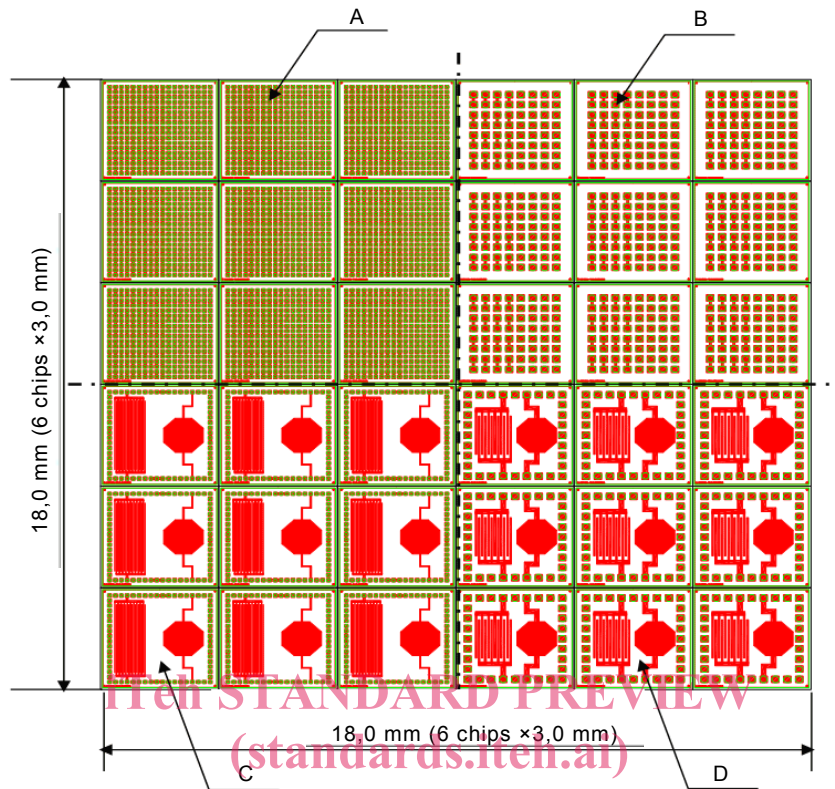
b) Detail of comb pattern

Specification of TEG-B 150 μm pitch chip

Name: SIPOS-TEG SB0601	Chip size: 3,0 mm × 3,0 mm
Pad pitch: 150 μm	Number of pads: 68
Pad size: 100 μm × 100 μm (aluminium wiring)	Pad opening: $\varphi = 90 \mu\text{m}$ (pad opening)
Size of comb pattern: L/S = 20 μm/20 μm	Number of comb patterns: 20 (10 × 2)
Dimension of inter-layer insulation pattern:	$\varphi = 1,0 \text{ mm}$ (octagonal)

**Figure 2 – Area array arrangement – TEG for insulation measurement of resistance between conductors and insulation resistance between layers**

Figure 3 and Figure 4 show chip arrangement in a shot and shot arrangement in a wafer, respectively.



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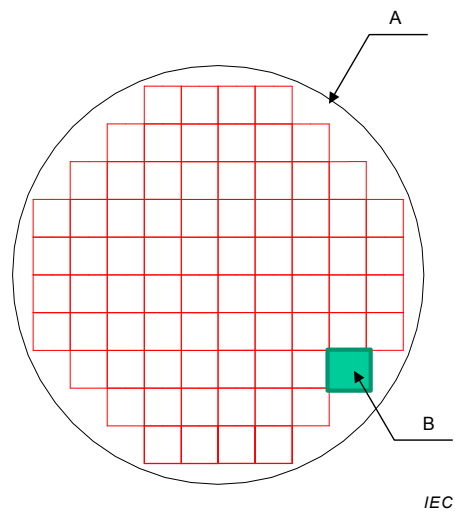
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**Key**

A	Area arrangement: TEG-A of 150 μm pad pitch
B	Area arrangement: TEG-A of 300 μm pad pitch
C	Area arrangement: TEG-B of 150 μm pad pitch
D	Area arrangement: TEG-B of 300 μm pad pitch

**Figure 3 – Chip arrangement in a shot**

**Key**

A	Wafer
B	Shot

Shot size: 18,0 mm × 18,0 mm

Number of shots: 76 shots per wafer (8 in (203,2 mm) wafer)

### Figure 4 – Shot arrangement in a wafer

Figure 5 shows the pitch chip specification of peripheral terminal of 60 μm TEG. Details of the peripheral terminal and interconnection are shown in Figure 6.

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